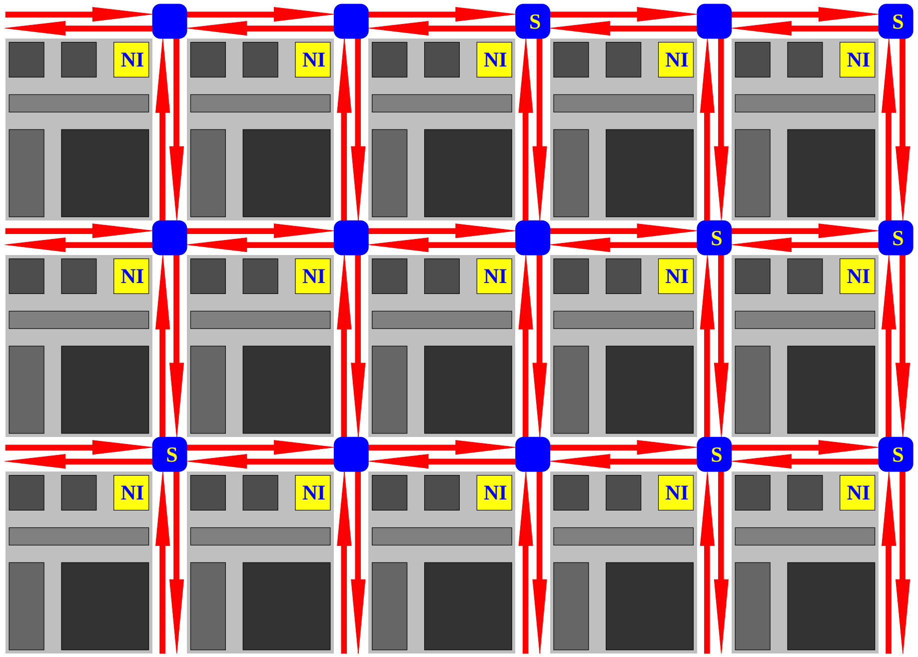
Resource Allocation for Quality of Service On-chip Communication



Axel Jantsch, Zhonghai Lu

Royal Institute of Technology, Stockholm

April 2008

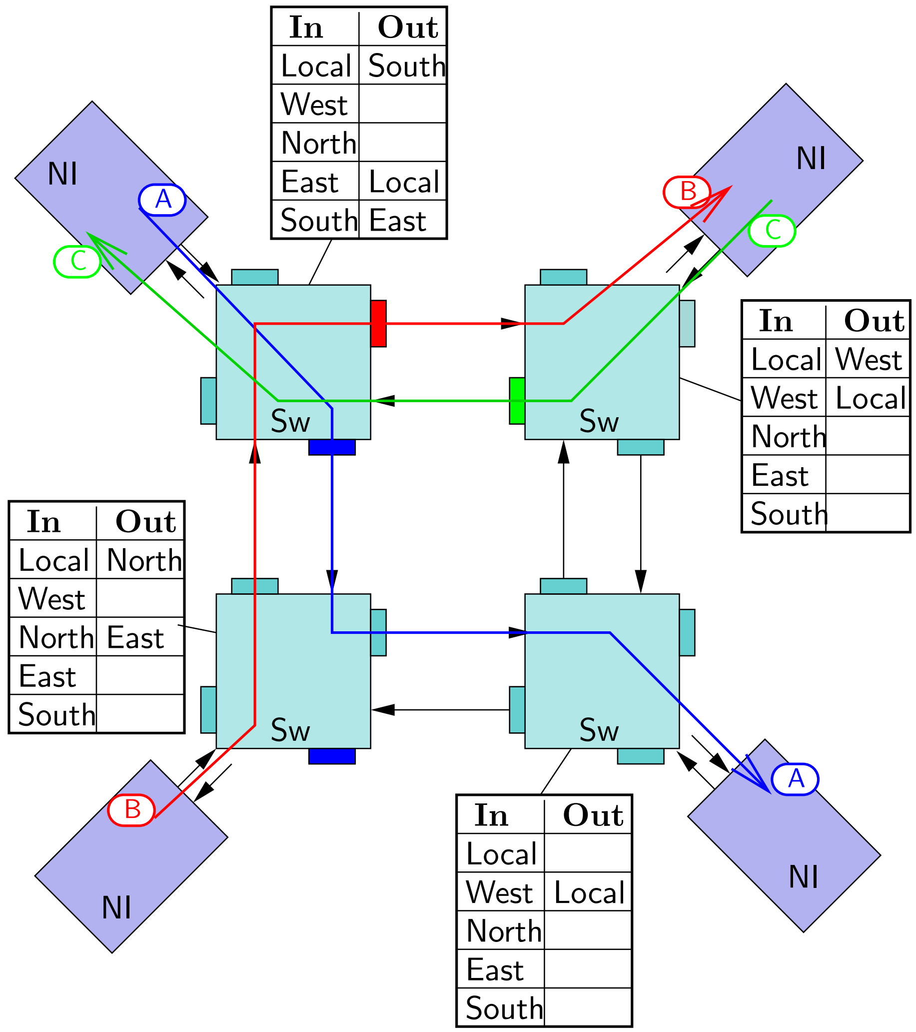
Overview

Circuit Switching

Time Division Multiplexing Virtual Circuits

Aggregate Resource Allocation

Circuit Switching



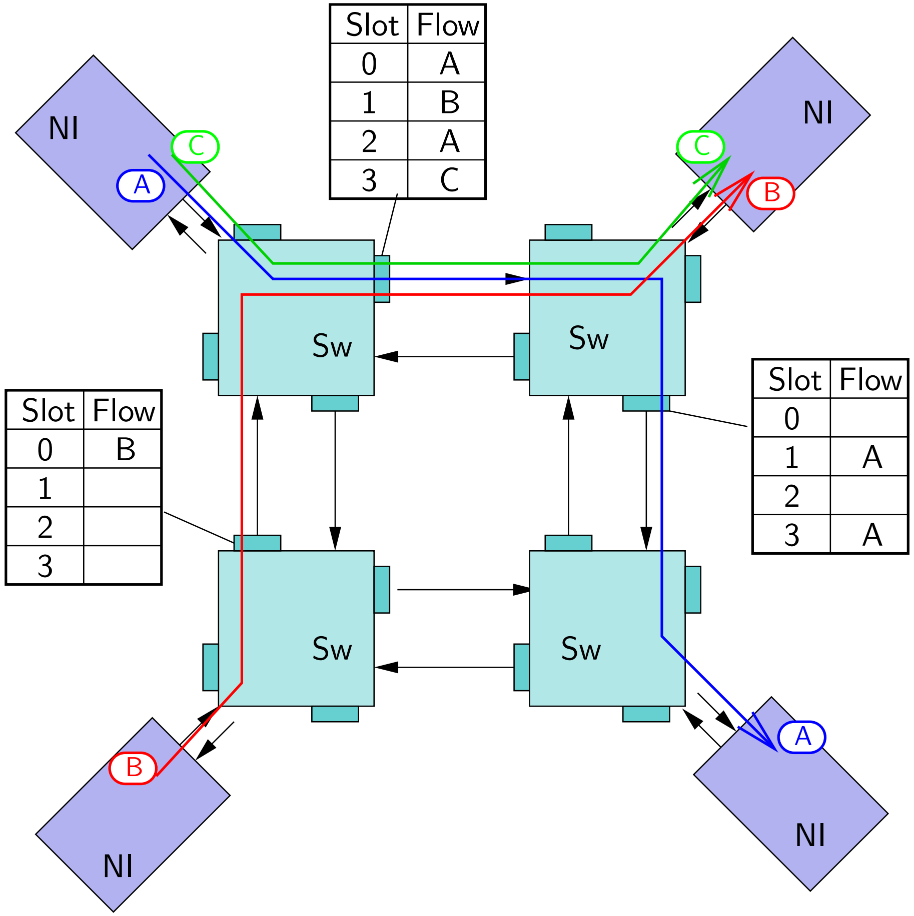
In	Out
Local	South
West	
North	
East	Local
South	East

In	Out
Local	West
West	Local
North	
East	
South	

In	Out
Local	North
West	
North	East
East	
South	

In	Out
Local	
West	Local
North	
East	
South	

Time Division Multiplexing - TDM

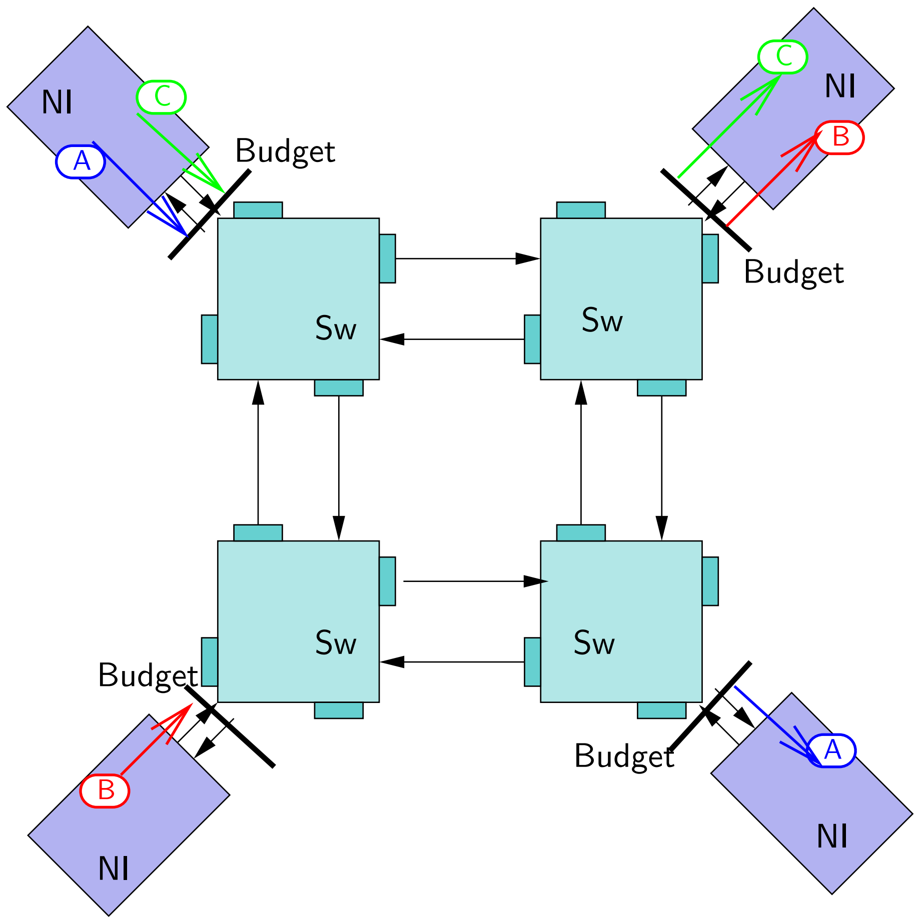


Slot	Flow
0	A
1	B
2	A
3	C

Slot	Flow
0	B
1	
2	
3	

Slot	Flow
0	
1	A
2	
3	A

Aggregate Traffic Budgets



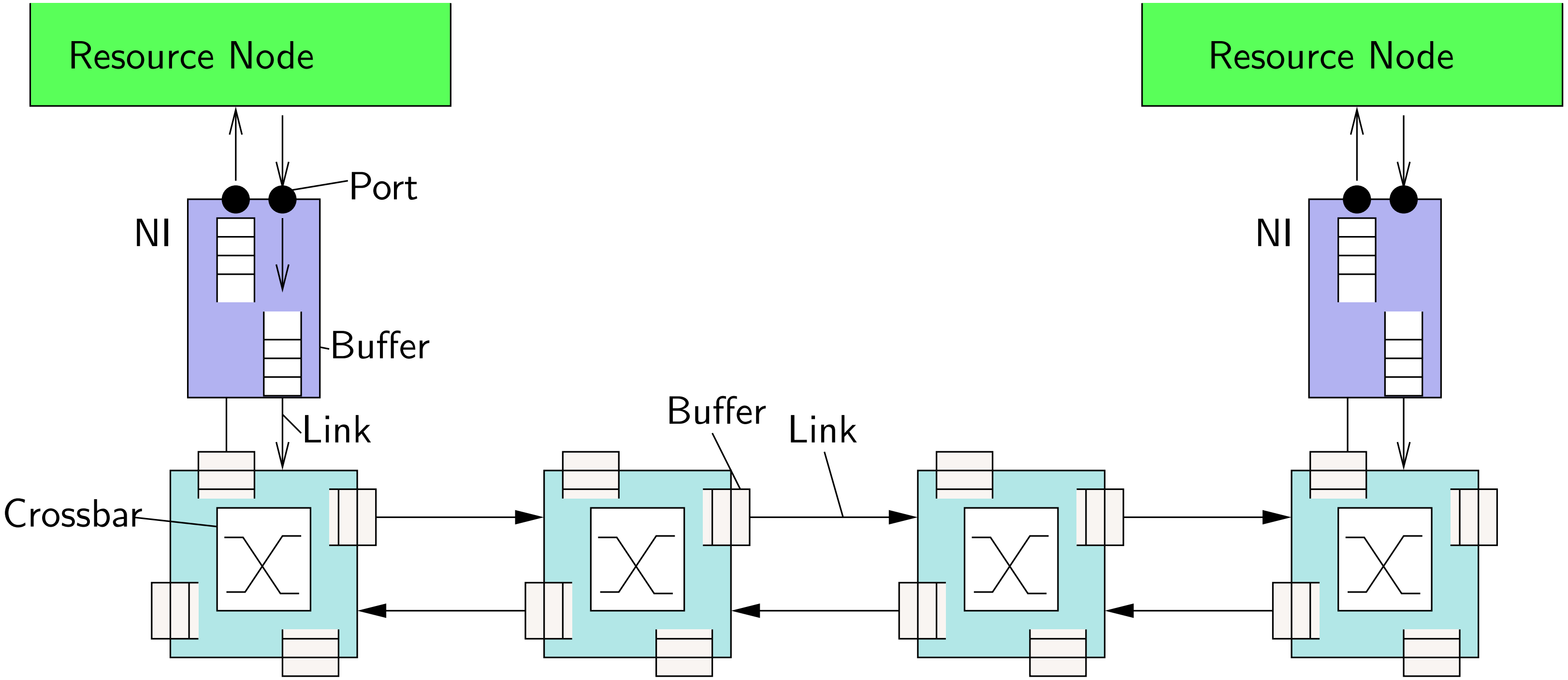
Overview

Circuit Switching

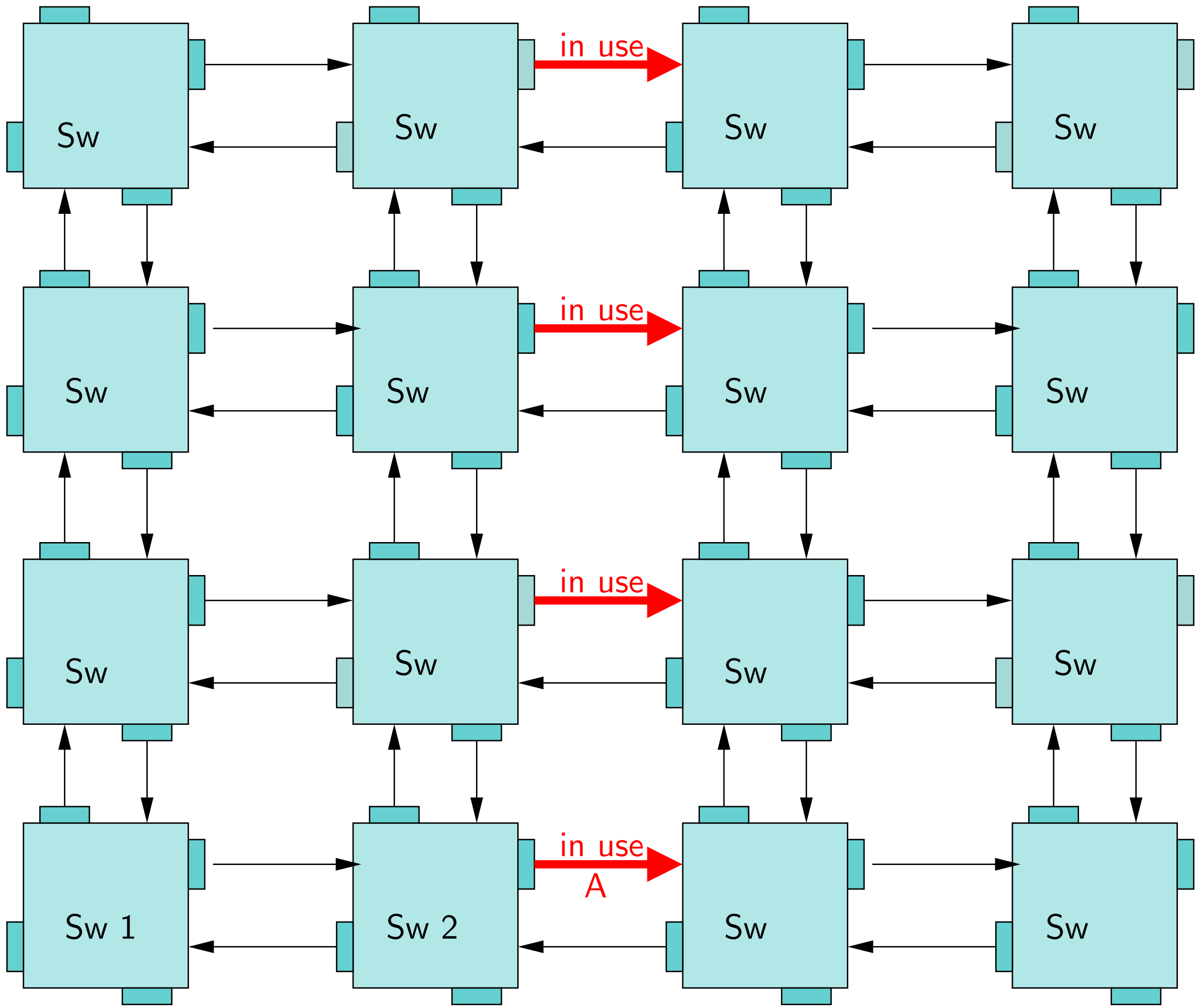
Time Division Multiplexing Virtual Circuits

Aggregate Resource Allocation

Circuit Switching - Resource Chain



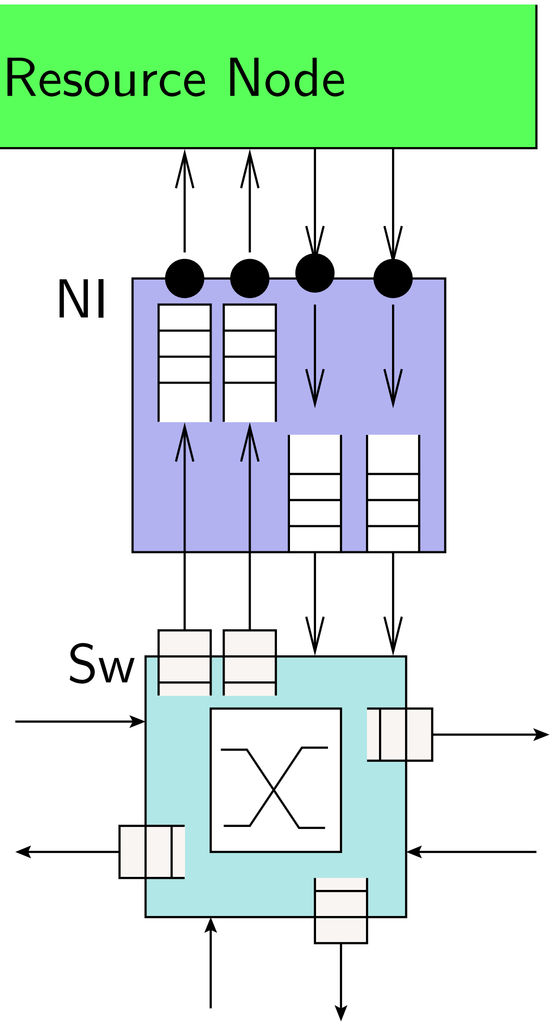
Circuit Switching Inflexibilities



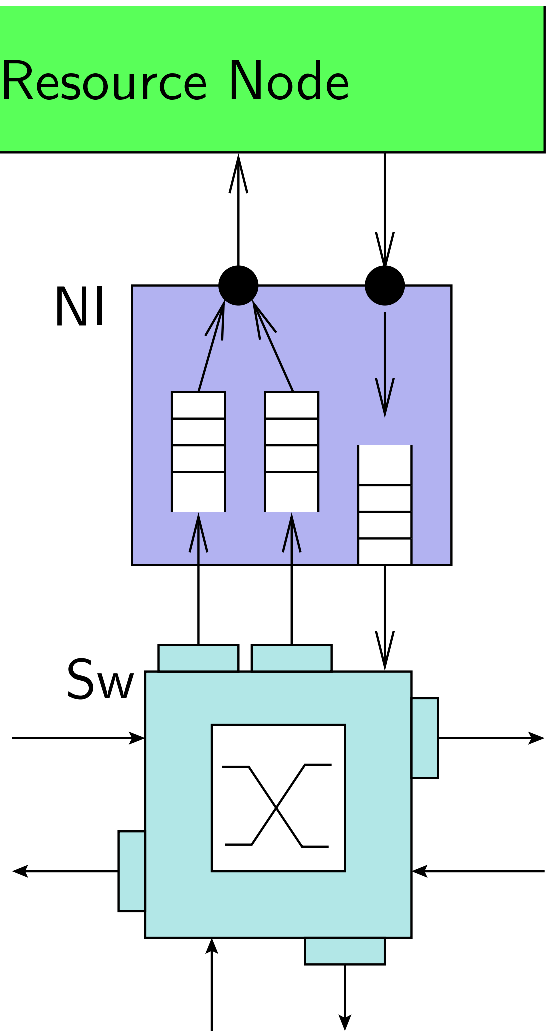
Pure Circuit Switching Can Be Beneficial

- Few static, well understood traffic streams with high throughput demands and long lifetime
- Networks with up to two hops

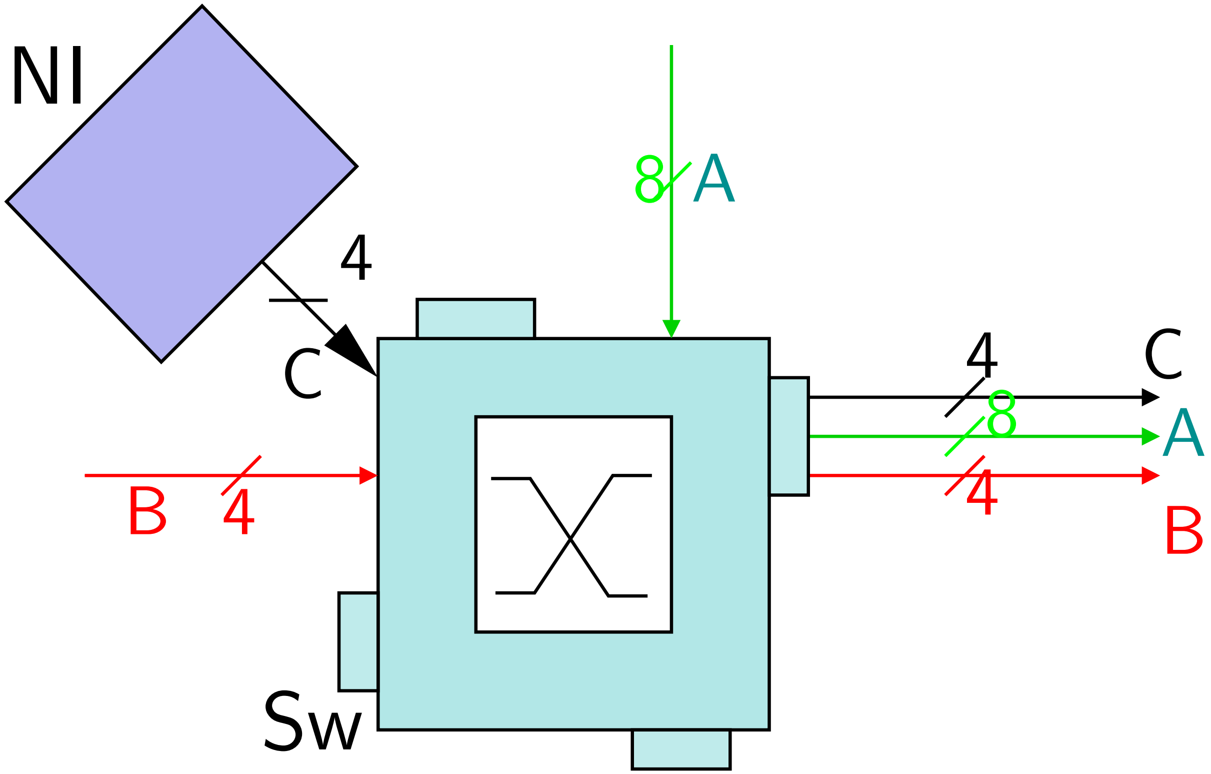
Circuit Switching - Duplication of NI Buffers



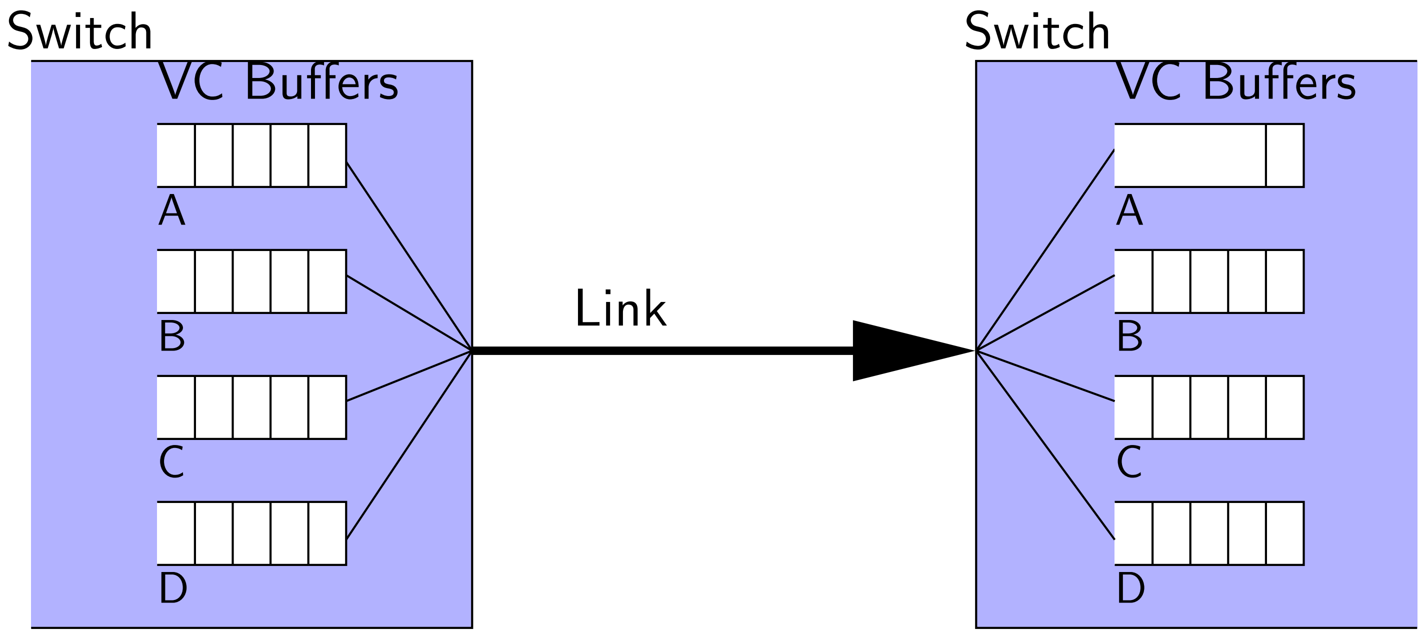
Circuit Switching - Dual Packet Exit



Circuit Switching with Spatial Division Multiplexing



Circuit Switching with Shared Links a lá Mango



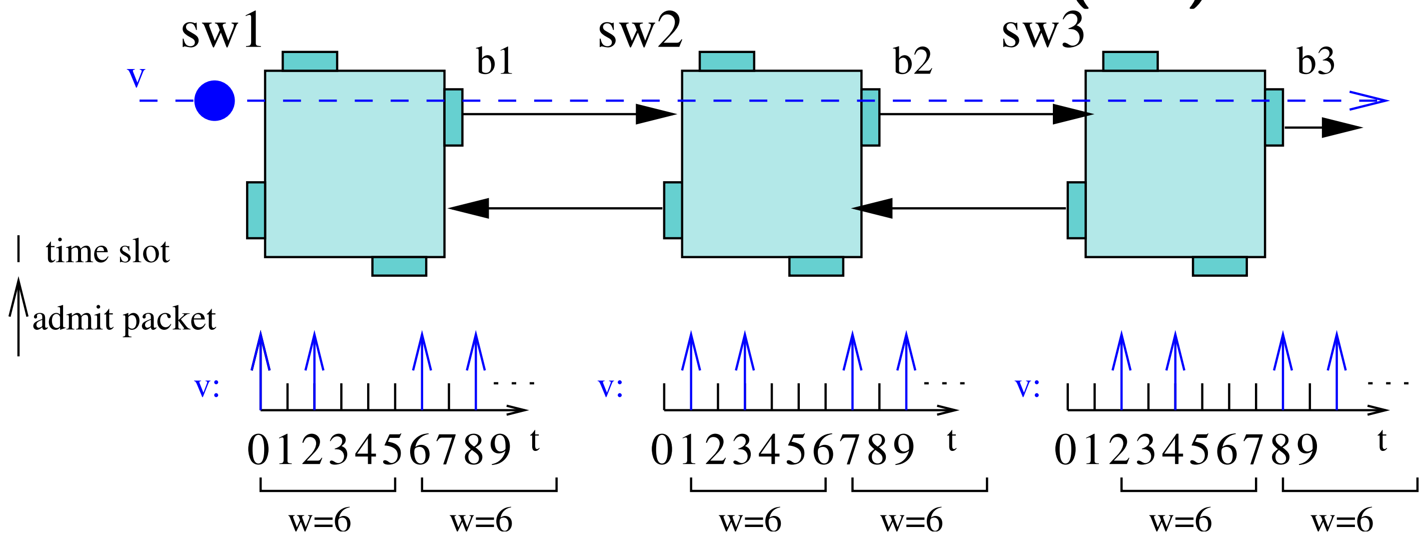
Overview

Circuit Switching

Time Division Multiplexing Virtual Circuits

Aggregate Resource Allocation

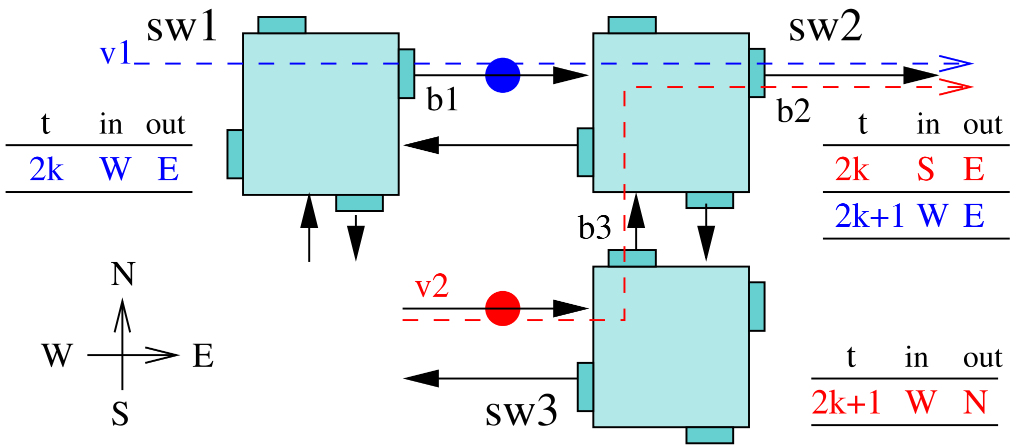
TDM Based Virtual Circuit (VC)



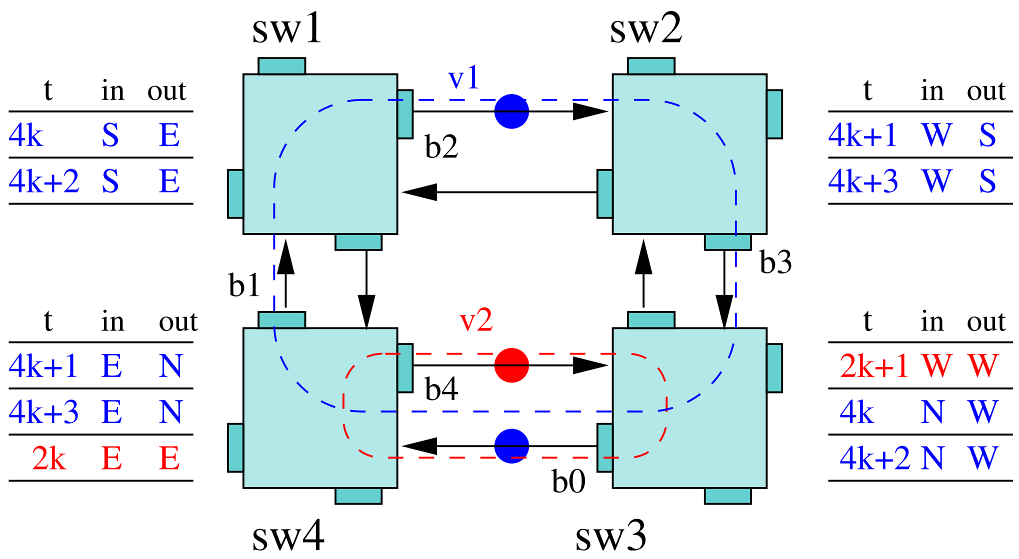
- Network is synchronized by a global time
- Links and buffers are allocated together
- VCs are defined by routing tables in switches
- Transmission speed is 1 hop/cycle
- Repetitive traffic papper is called an admission cycle (e.g. 2 packets per 6 slots
- Buffer occupation:
  - ⋆ b_1: slots 0, 2, 6, 8, 12, 14, ...
  - ⋆ b_2: slots 1, 3, 7, 9, 13, 15, ...
  - ⋆ b_1: slots 2, 4, 8, 10, 14, 16, ...

Open Ended and Closed Loop VCs

Æthérial:



Nsotrum:



TDM VC Configuration Problem

Given a set of VC specifications (source, destination, minimum bandwidth), determine and implement the necessary VCs.

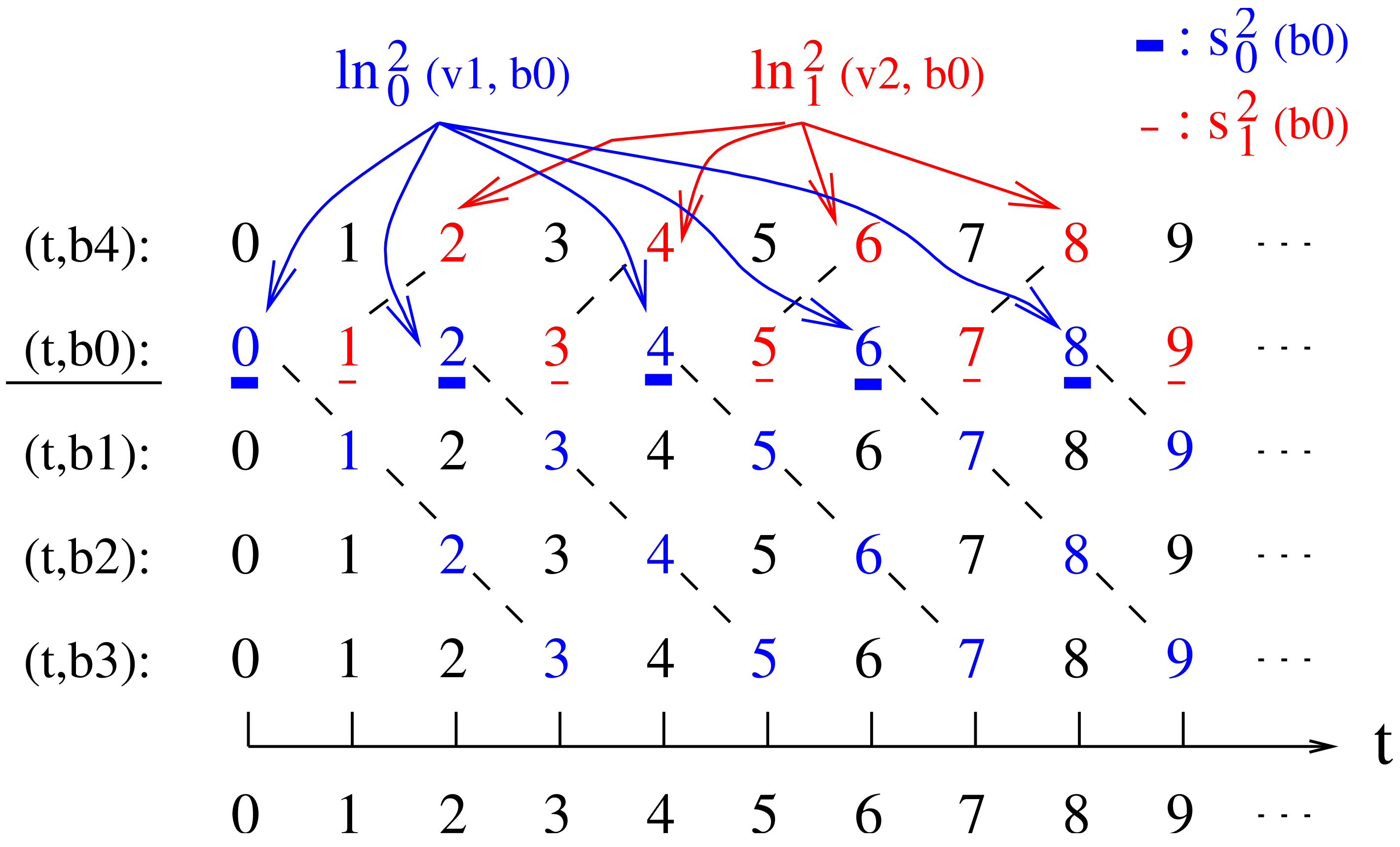
- Path selection: For each VC determine the sequence of nodes between source and destination.
- Slot allocation: For each VC determine the allocated time slots for each buffer in the VC.

Conditions to be satisfied:

- All VCs are contention free;
- All VCs allocated sufficient number of slots to provide the require bandwidth;
- The network must be deadlock free and livelock free;
- Sufficient bandwidth must remain for best effort traffic;

Logic Networks

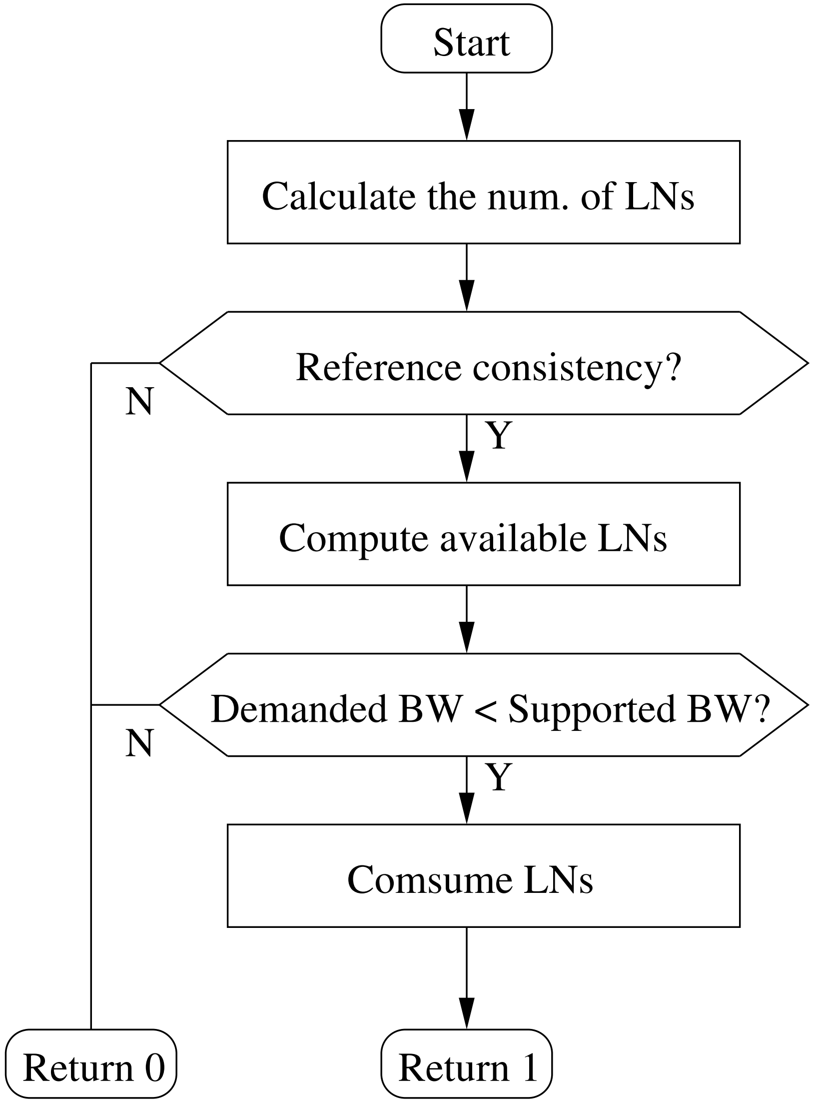
A logic network (LN) is an infinite set of associated *(time slot, buffer)* pairs with respect to a buffer on a path.



Logic Network Properties

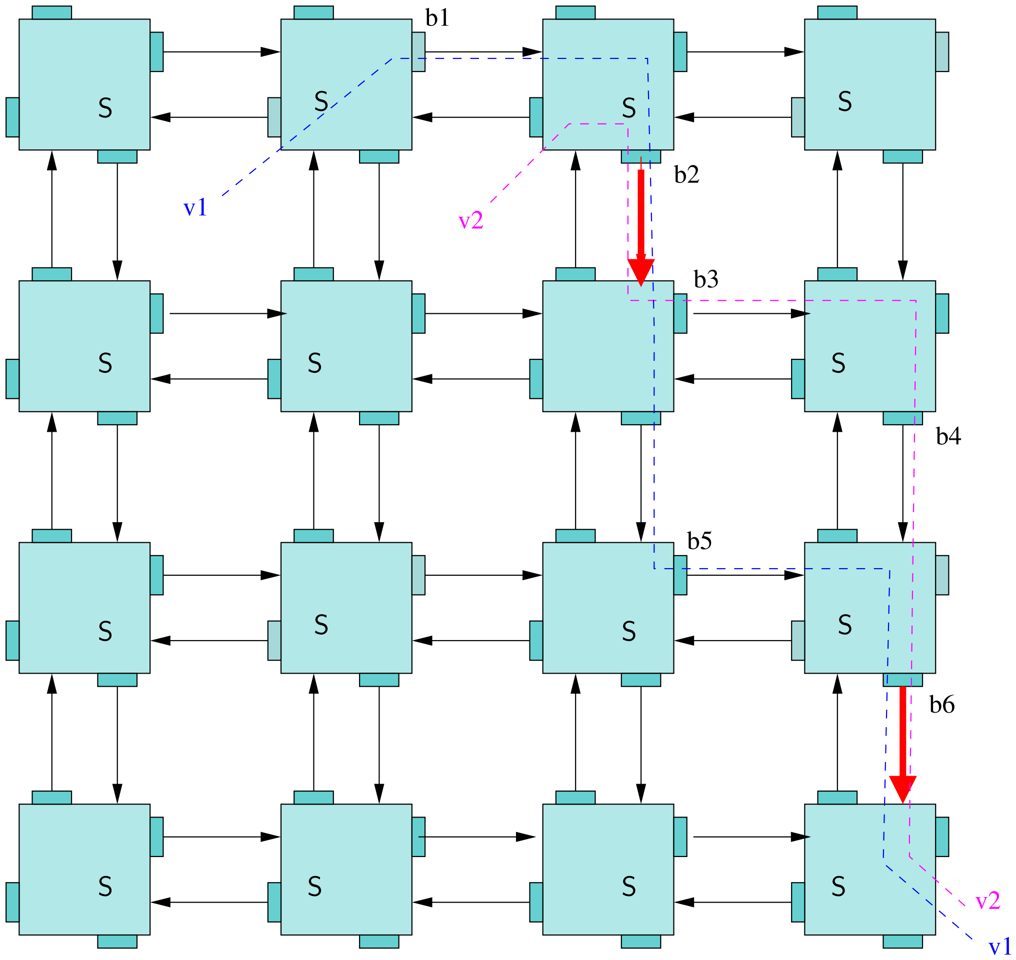
- The maximum number N of LNs that can be constructed such, that two VCs v_1 and v_2 subscribe to different LNs without conflict, is $\gcd(D_1, D_2) \geq N$ (D_1 and D_2 are admission cycles of v_1 and v_2); The bandwidth of an LN is $1/N$ packet/cycle.
- Assigning v_1 and v_2 to different LNs is sufficient and necessary to avoid conflict;
- If v_1 and v_2 have multiple shared buffers, they need to be *reference consistent*; reference consistency can be checked linearly;

Logic Network based Slot Allocation



Slot Allocation Example

- $v_1 = b_1, b_2, b_5, b_6, BW(v_1) = 3/8$,
  $v_2 = b_2, b_3, b_4, b_6, BW(v_2) = 7/16$,
- $N = GCD(8, 16) = 8$
- Shared buffers are b_2 and b_6
- Distance between b_2 and b_6 is 2 along both v_1 and v_2 $\Rightarrow$ Buffers are reference consistent
- With b_2 as reference buffer we have as slot set: $0, 1, 2, 3, 4, 5, 6, 7$, each represents an LN
- We allocate slots $0, 2, 4 \rightarrow v_1$; $1, 3, 5, 7 \rightarrow v_2$;



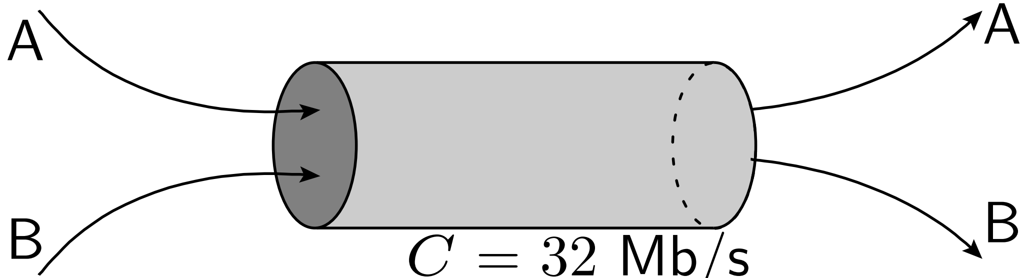
Overview

Circuit Switching

Time Division Multiplexing Virtual Circuits

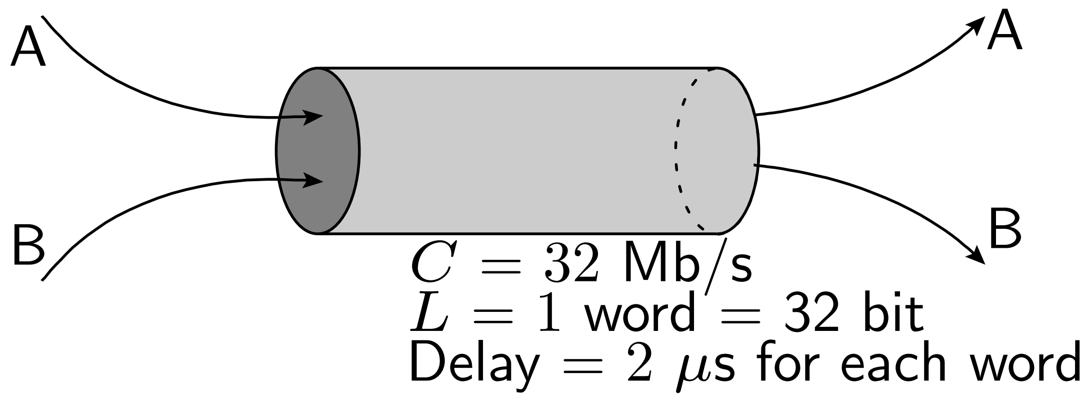
Aggregate Resource Allocation

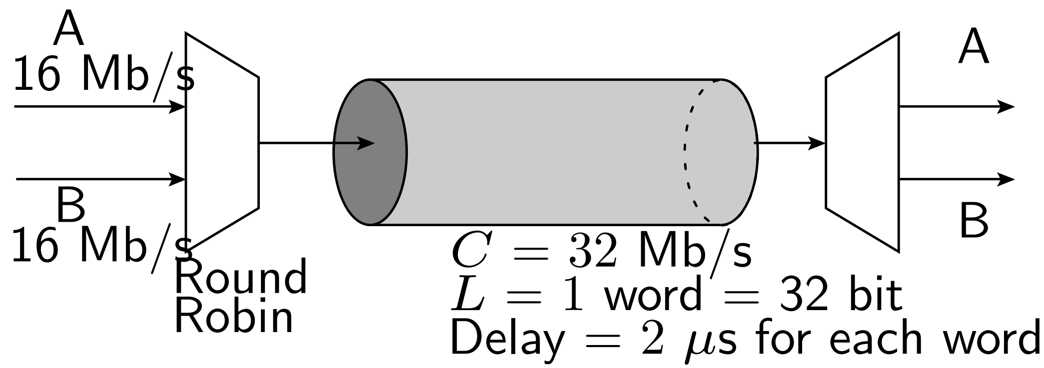
Aggregate Allocation of a Channel



$C = 32$ Mb/s
$L = 1$ word $= 32$ bit
Delay $= 2\ \mu$s for each word

Aggregate Allocation of a Channel





- Characteristics of the flows
- Arbitration policy for channel access

(σ, ρ) **Regulated Flows**

A Flow F is (σ, ρ) regulated if

$$F(b) - F(a) \leq \sigma + \rho(b - a)$$

for all time intervals $[a, b], 0 \leq a \leq b$ and where
$F(t) \cdots$ the cumulative amount of traffic between 0 and $t \geq 0$.
$\sigma \geq 0$ is the burstiness constraint;
$\rho \geq 0$ is the maximum average rate;

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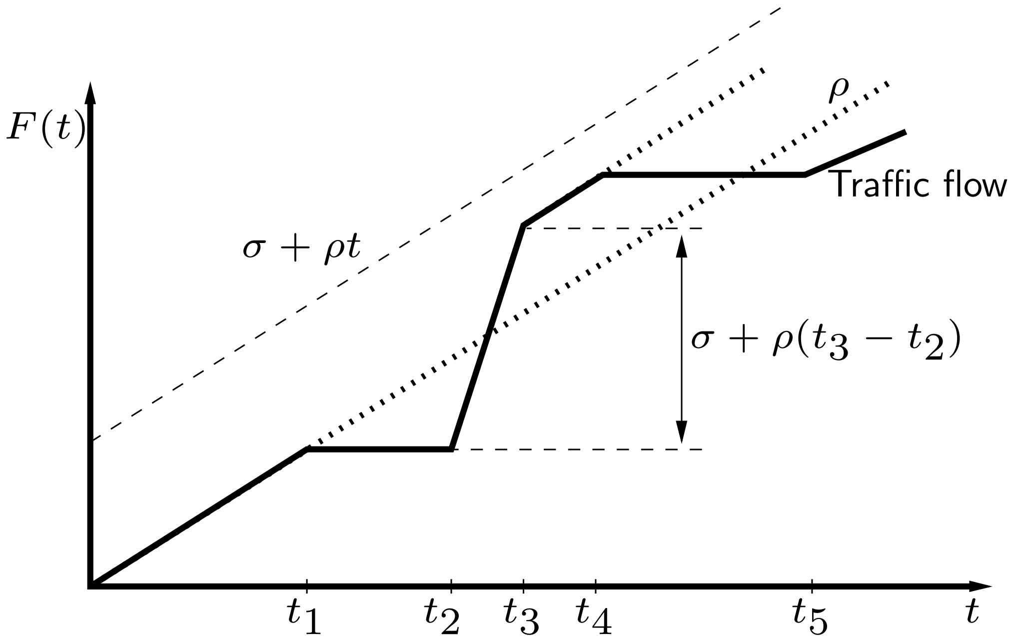
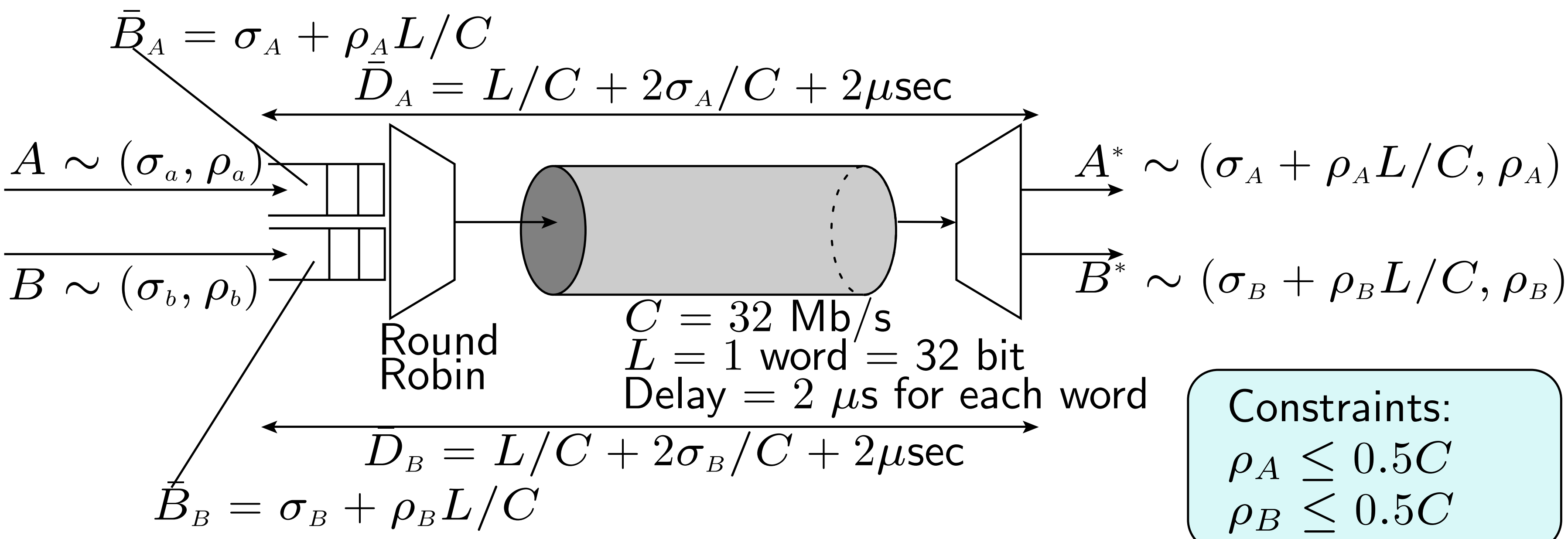


Channel Shared by Two Regulated Flows - Round Robin



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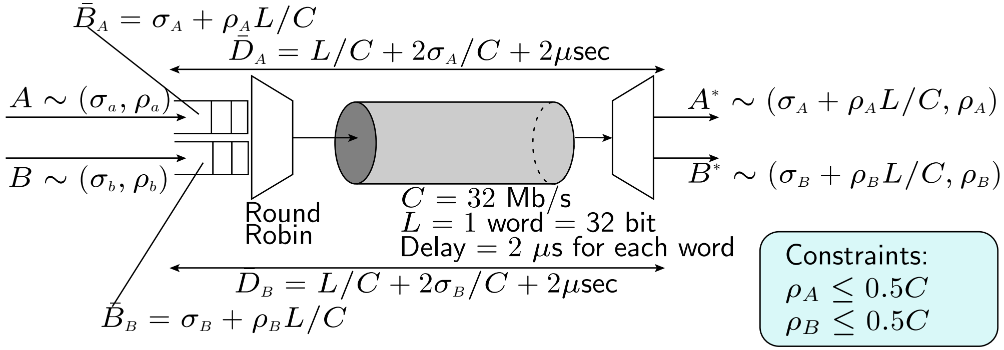
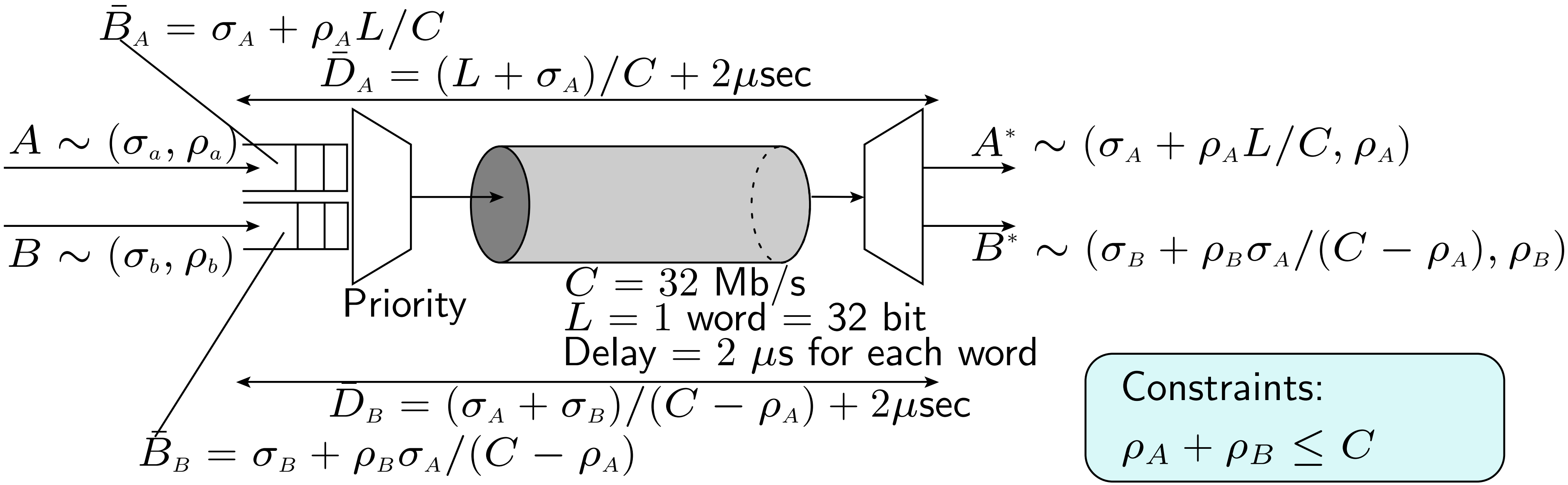


A	B	A			B		
(σ_A, ρ_A)	(σ_B, ρ_B)	$\bar{B}_A$	$\bar{D}_A$	$(\sigma_{A^*}, \rho_{A^*})$	$\bar{B}_B$	$\bar{D}_B$	$(\sigma_{B^*}, \rho_{B^*})$
$(0, 16.00)$	$(0, 16.00)$	32	3	$(32, 16.00)$	32	3	$(32, 16.00)$
$(0, 12.80)$	$(0, 12.80)$	32	3	$(32, 12.80)$	32	3	$(32, 12.80)$
$(0, 9.60)$	$(0, 16.00)$	32	3	$(32, 9.60)$	32	3	$(32, 16.00)$
$(0, 6.40)$	$(0, 16.00)$	32	3	$(32, 6.40)$	32	3	$(32, 16.00)$
$(0, 3.20)$	$(0, 16.00)$	32	3	$(32, 3.20)$	32	3	$(32, 16.00)$
$(0, 16.00)$	$(0, 16.00)$	32	3	$(32, 16.00)$	32	3	$(32, 16.00)$
$(32, 16.00)$	$(0, 16.00)$	64	5	$(64, 16.00)$	32	3	$(32, 16.00)$
$(64, 16.00)$	$(0, 16.00)$	96	7	$(96, 16.00)$	32	3	$(32, 16.00)$
$(128, 16.00)$	$(0, 16.00)$	160	11	$(160, 16.00)$	32	3	$(32, 16.00)$
$(256, 16.00)$	$(0, 16.00)$	288	19	$(288, 16.00)$	32	3	$(32, 16.00)$

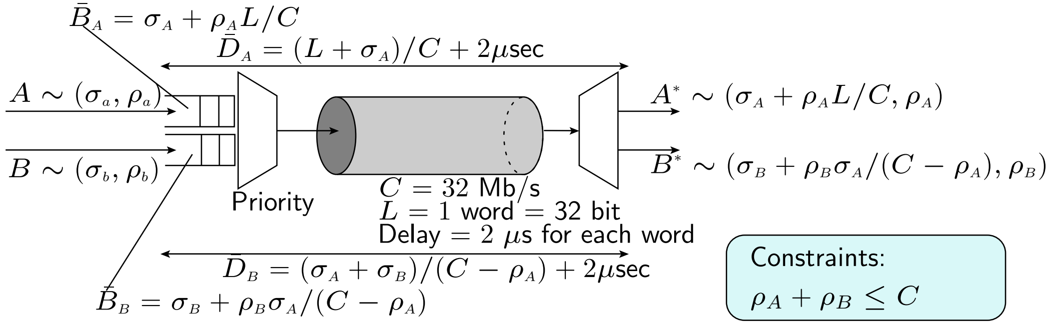
Channel Shared by Two Regulated Flows - Priority



Constraints:

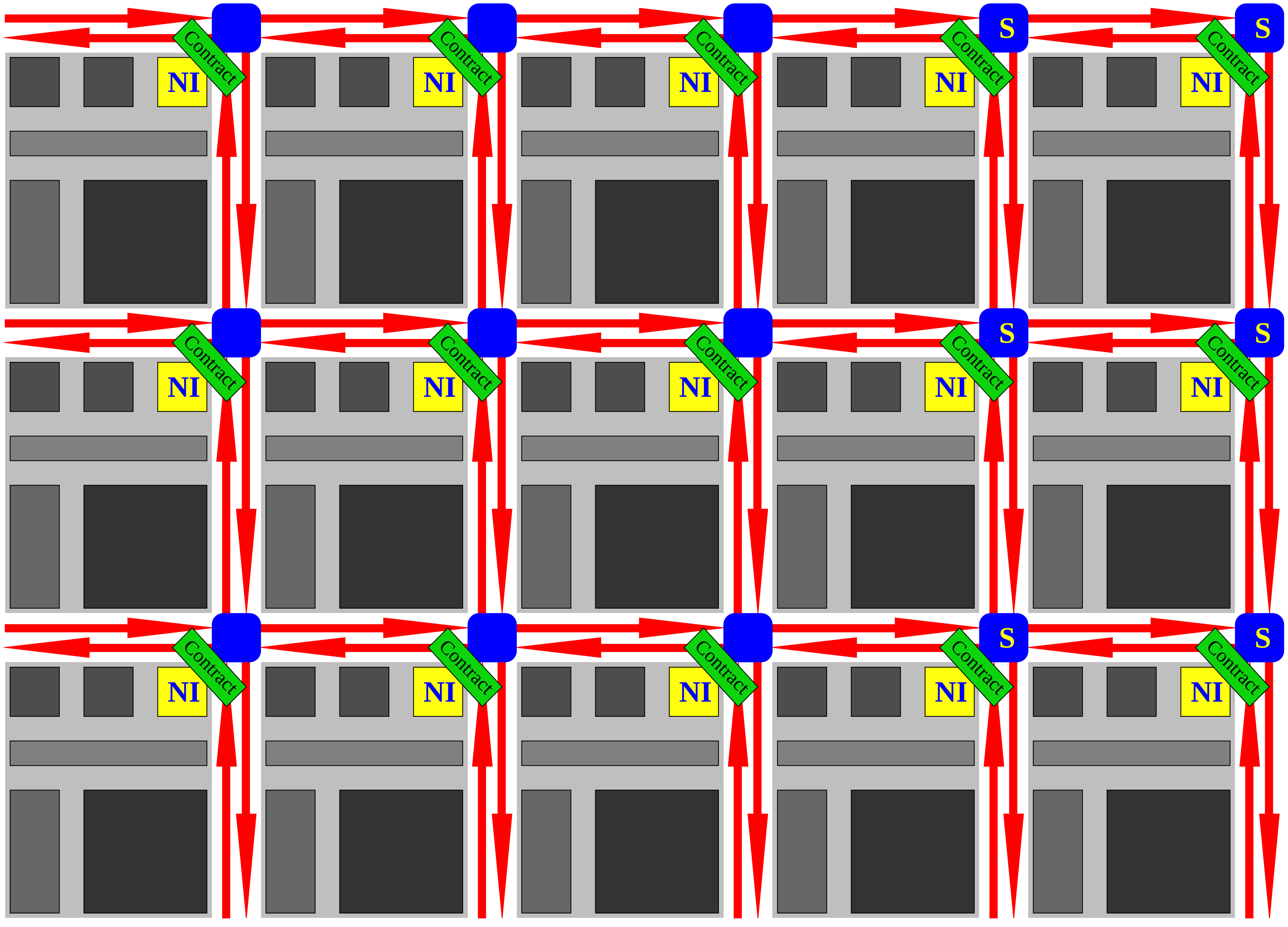
$\rho_A + \rho_B \leq C$

Aggregate Allocation of a Channel



A	B	A			B		
(σ_A, ρ_A)	(σ_B, ρ_B)	$\bar{B}_A$	$\bar{D}_A$	$(\sigma_{A^*}, \rho_{A^*})$	$\bar{B}_B$	$\bar{D}_B$	$(\sigma_{B^*}, \rho_{B^*})$
$(0, 16.00)$	$(0, 16.00)$	32	3	$(32, 16.00)$	32	4	$(32, 16.00)$
$(0, 12.80)$	$(0, 12.80)$	32	3	$(32, 12.80)$	32	4	$(32, 12.80)$
$(0, 9.60)$	$(0, 16.00)$	32	3	$(32, 9.60)$	32	3	$(32, 16.00)$
$(0, 6.40)$	$(0, 16.00)$	32	3	$(32, 6.40)$	32	3	$(32, 16.00)$
$(0, 3.20)$	$(0, 16.00)$	32	3	$(32, 3.20)$	32	3	$(32, 16.00)$
$(0, 16.00)$	$(0, 16.00)$	32	3	$(32, 16.00)$	32	4	$(32, 16.00)$
$(32, 16.00)$	$(0, 16.00)$	64	4	$(64, 16.00)$	32	4	$(32, 16.00)$
$(64, 16.00)$	$(0, 16.00)$	96	5	$(96, 16.00)$	64	6	$(64, 16.00)$
$(128, 16.00)$	$(0, 16.00)$	160	7	$(160, 16.00)$	128	10	$(128, 16.00)$
$(256, 16.00)$	$(0, 16.00)$	288	11	$(288, 16.00)$	256	18	$(256, 16.00)$

Aggregate Resource Allocation for the Entire Network



Aggregate Resource Allocation In Nostrum

$$\begin{aligned}
\sum_{h \in H_r^o} E_h &\leq B_r^o \\
\sum_{h \in H_r^i} E_h &\leq B_r^i \\
\sum_r B_r^o = \sum_r B_r^i &\leq \kappa C_{\mathsf{Net}} \\
\mathrm{BW}_h &= \frac{n_h}{W} \\
\mathrm{maxLat}_h &= 5DN \\
\mathrm{avgLat}_h &= d_h \delta
\end{aligned}$$

Summary

- QoS Provision is about resource allocation
- Circuit switching
- Time Division Multiplexing
- Aggregate resource allocation
- Exclusive allocation - shared resources
- Average case - worst case
- Allocation flexibility - cost efficiency