

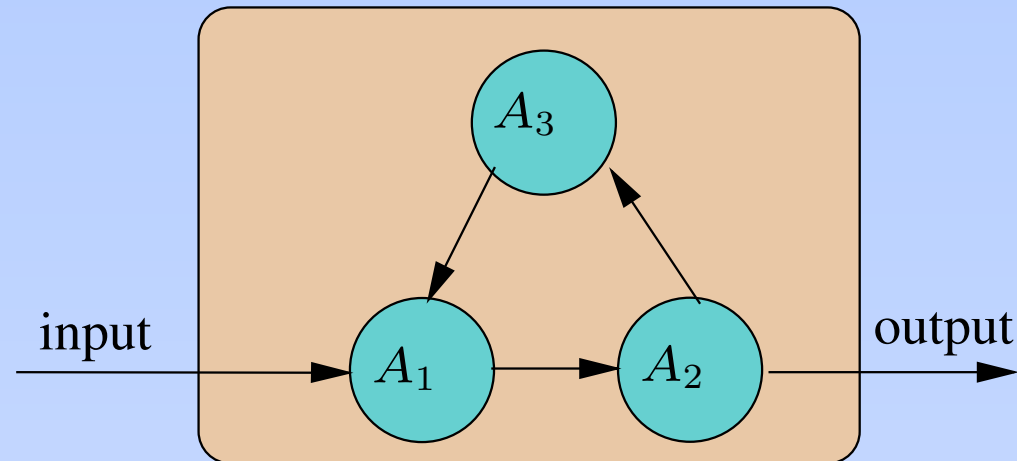
# ForSyDe: A Denotational Framework for Heterogeneous Models of Computation

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Models of Computation and Communication  
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# ForSyDe Features



## Processes

- Communicate through signals only;
- Functional
- State-full
- Blocking read
- Partition input and output signals
- Evaluate when required input is available

## Signals:

- Sequences of events
- Preserve event order
- Have one writer and multiple readers
- Untimed MoC: Events are partially ordered
- Discrete Time MoCs: Signals carry timing information

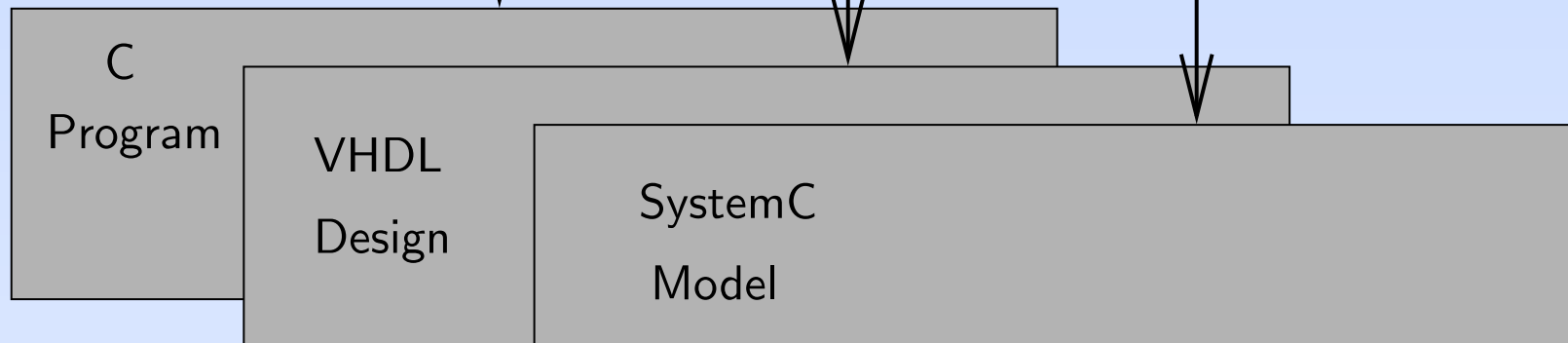
# The ForSyDe Design Flow

## Ideal System Model

No resource limitation on  
processors  
communication bandwidth and delay  
memory

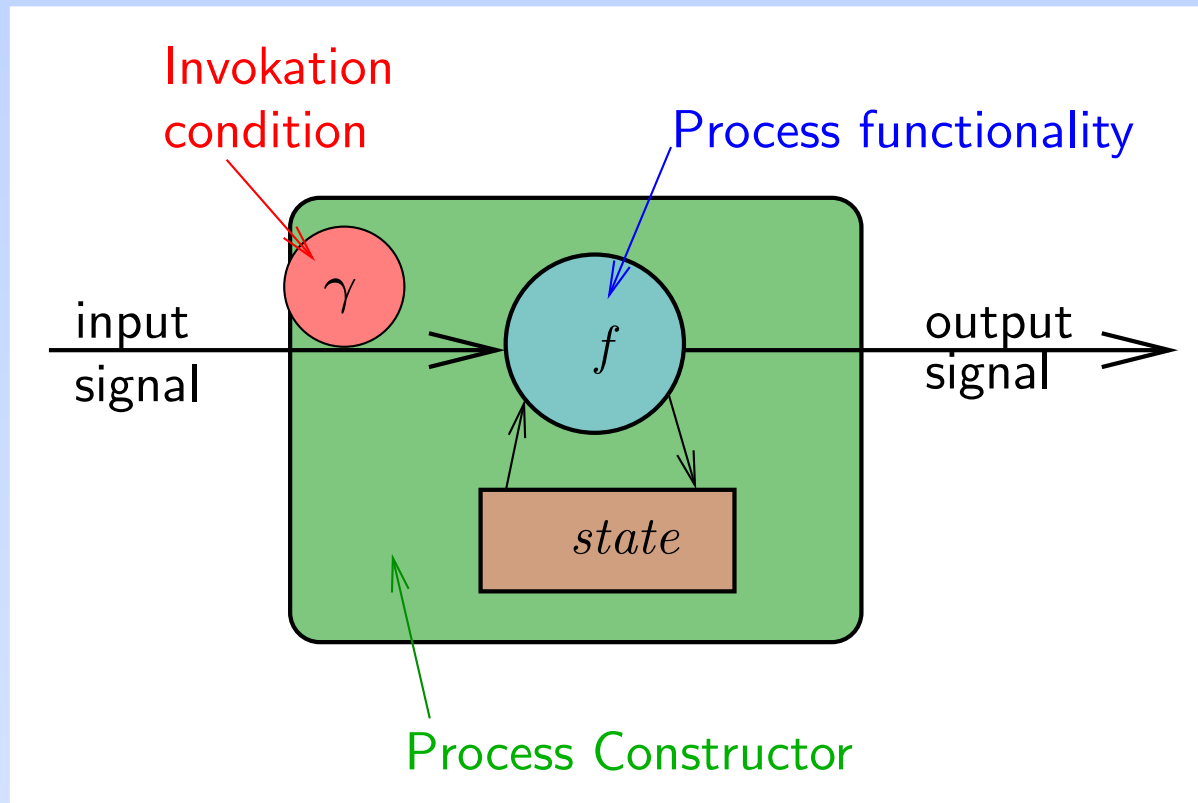
## Implementation Model

with Finite resources  
processors, HW blocks,  
reconfigurable resources  
buffers  
communication architecture  
schedulers, arbiters

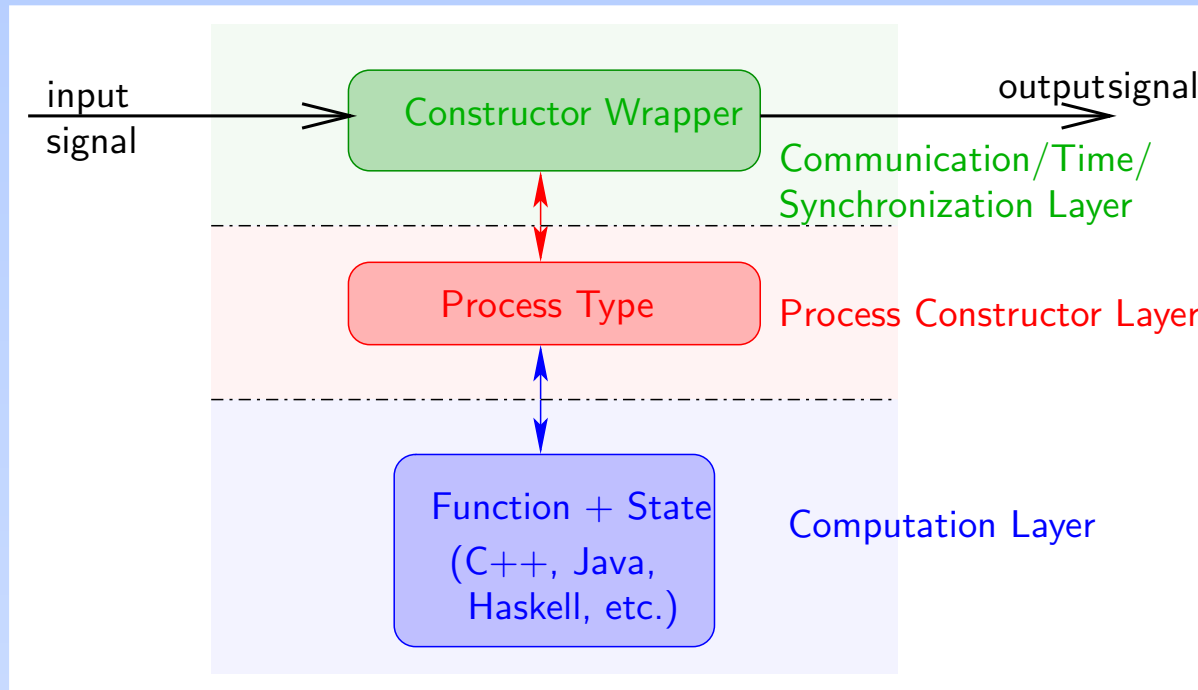


# Process Constructors

process = constructor + function + initial\_state + invokation\_condition



# Layered View of Process Constructors



## Models of Computation

- Untimed MoC (Datflow, SDF, Rendezvous)
- Synchronous MoC (Perfectly, Clocked)
- Discrete Time MoC
- Soon: Continuous Time MoC

## Process Combinators

- Sequential Composition
- Parallel Composition
- Feed-back Composition

## Process Constructor Types

- State-less Processes
- FSM Machines
- Zip / Unzip Processes
- Sources and Sinks

# The $\text{map}U$ Process Constructor

$$\text{map}U(c, f) = p$$

where  $p(\dot{s}) = \dot{s}'$

$$f(\dot{a}_i) = \dot{a}'_i$$

$$\pi(\nu, \dot{s}) = \langle \dot{a}_i \rangle, \nu(i) = c$$

$$\pi(\nu', \dot{s}') = \langle \dot{a}'_i \rangle, \nu'(i) = \#f(\dot{a}_i)$$

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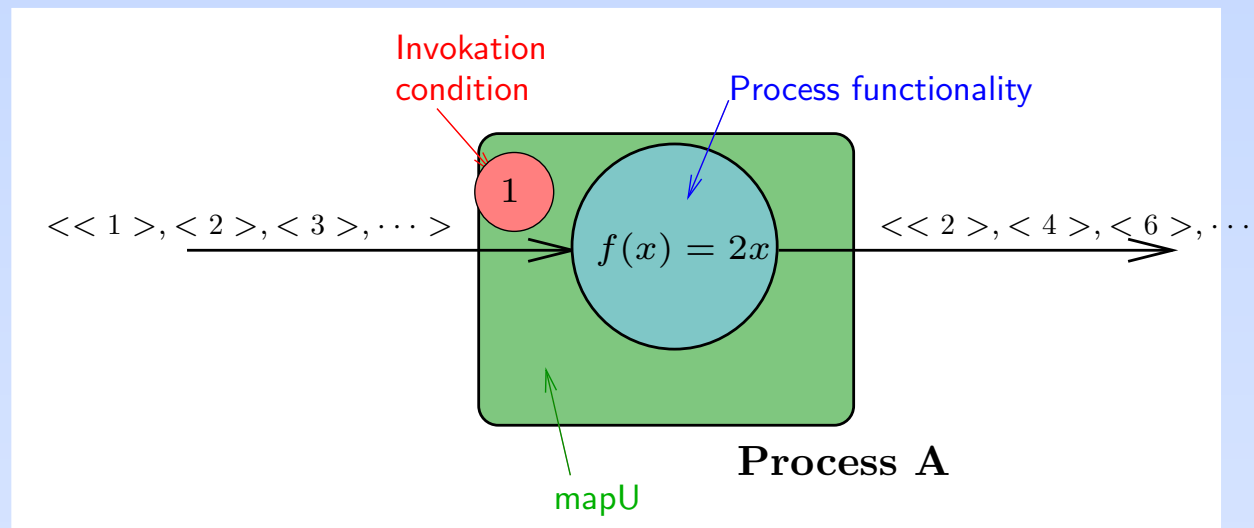
$$\pi(\nu, \dot{s}) = \langle \dot{a}_i \rangle, \nu(i) = c$$

$$\pi(\nu', \dot{s}') = \langle \dot{a}'_i \rangle, \nu'(i) = \#f(\dot{a}_i)$$

Example:

$$A = mapU(c, f)$$

where  $c = 1$   
 $f(x) = 2x$



# Definition of a Model of Computation

The **Untimed Model of Computation (Untimed MoC)** is defined as  $\text{Untimed MoC} = (C, O)$ , where

$$C = \{ \text{map}U, \text{scan}U, \text{scand}U, \text{mealy}U, \text{moore}U, \\ \text{zip}U, \text{zip}Us, \text{zipWith}U, \text{unzip}U, \\ \text{source}U, \text{sink}U, \text{init}U \}$$

$$O = \{ ||, \circ, \mathbf{FB}_P \}$$

- Synchronous Model of Computation
- Clocked Synchronous Model of Computation
- Discrete Time Model of Computation



# The Integrated MoC

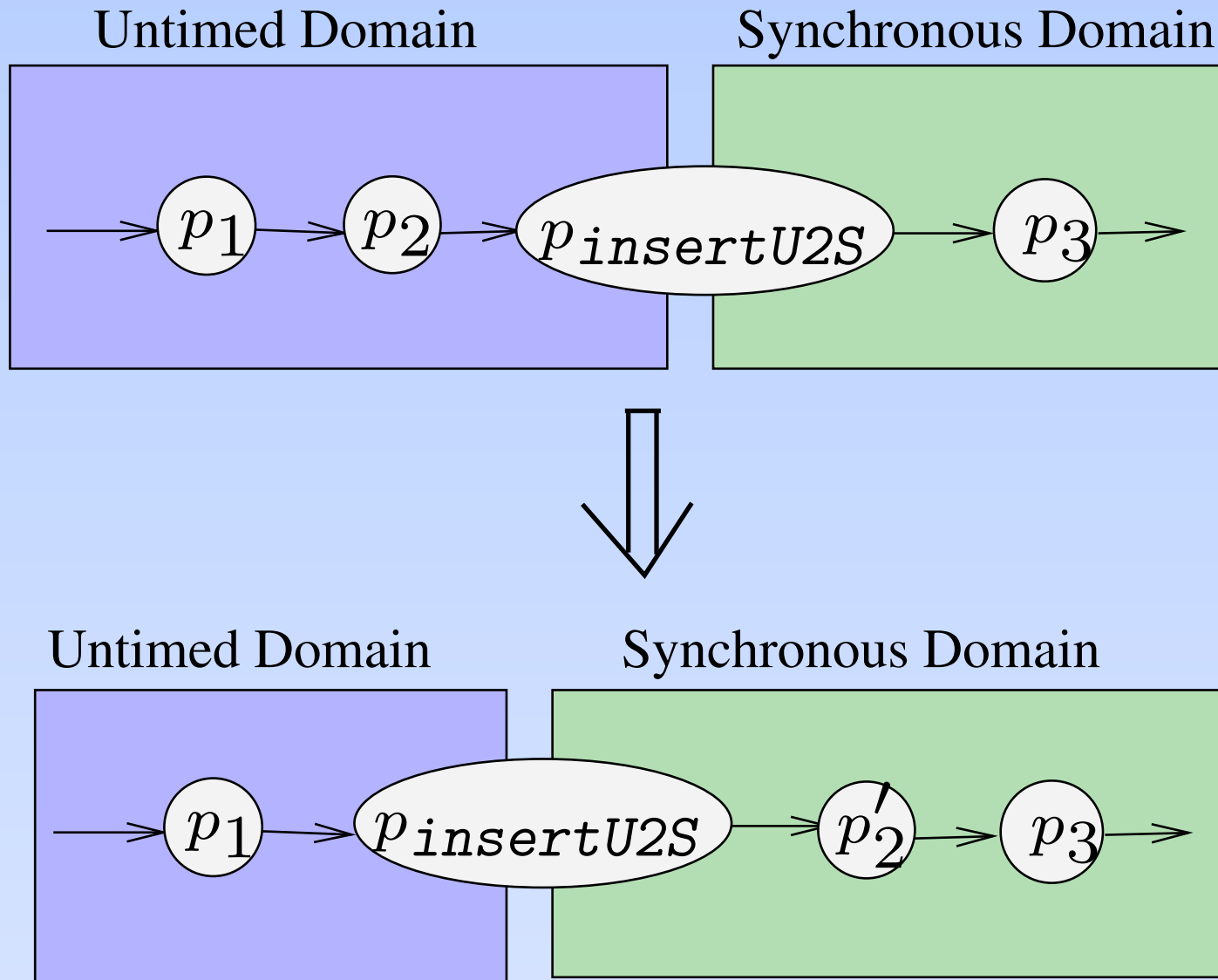
The **Integrated Model of Computation (Integrated MoC)** is defined as Integrated HMoC= $(M, C, O)$ , where

$$M = \{\text{U-MoC, S-MoC, CS-MoC, T-MoC}\}$$

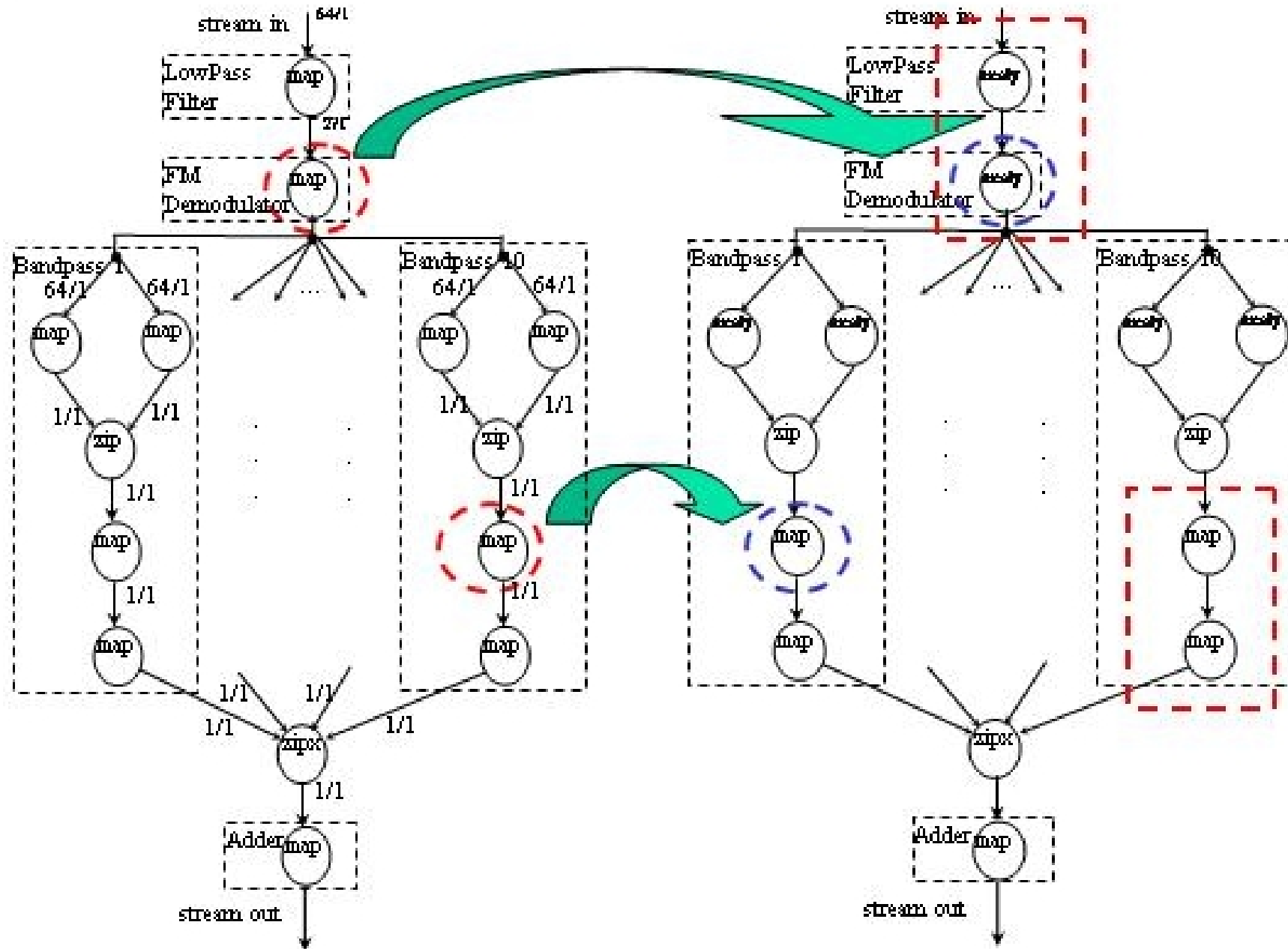
$$C = \{ \textit{intSup}, \textit{intSdown}, \textit{intTup}, \textit{intTdown}, \\ \textit{stripT2S}, \textit{stripT2U}, \textit{stripS2U}, \\ \textit{insertS2T}, \textit{insertU2T}, \textit{insertU2S} \}$$

$$O = \{ \parallel, \circ, \mathbf{FB}_P \}$$

# Process Migration



# Process Refinement - FM Software Radio Example



SDF Model

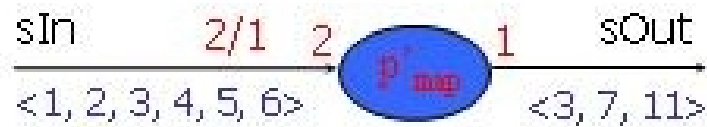
Synchronous Model

# Process Refinement - FM Software Radio Example

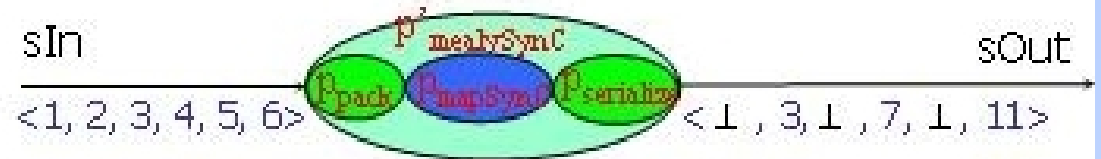
SDF domain

Synchronous domain

Communication layer:

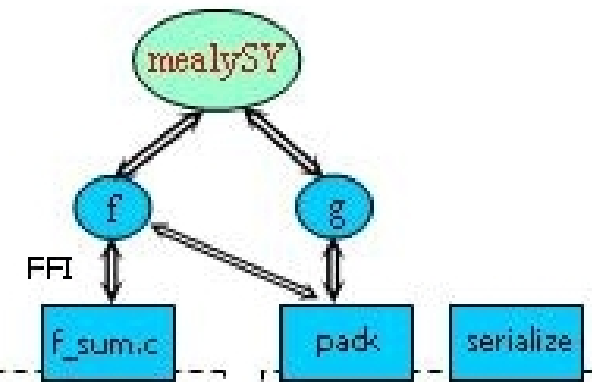
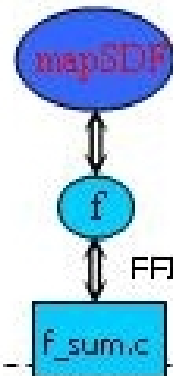


mapSDF f\_sum sIn = sOut



mealySY g f\_sum sIn = sOut

Computation layer:



Library of Algorithms:

```
// ***
// .....
// .....
```

```
// f_sum.c
int* sum(int *f1, int *f2) {
    *f2 += *f1;
    return f2; }
}
```

ForSyDe Library of pack & serialize:

```
- module pack
- module serialize
.....
```

## Transformation Rules - Scheduling



- A combinational process with  $m$  input signals is modeled with  $zipWithSY_m(f)$
- In each event cycle the function  $f$  is applied to the current values of the input signals
- A large amount of computational resources may be required for these processes

# Transformation Rules - Scheduling

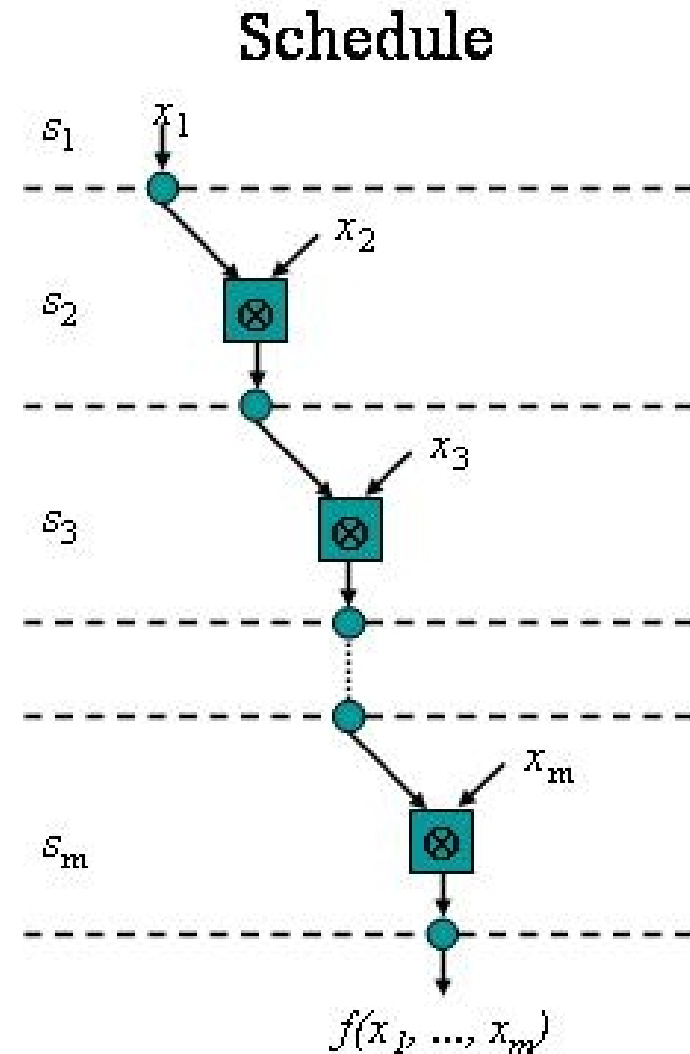
## Combinational process



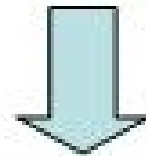
If

$$f(x_1, \dots, x_m) = x_1 \otimes x_2 \otimes \dots \otimes x_m$$

the following schedule using only one computational unit can be derived:



# Transformation Rules - Scheduling



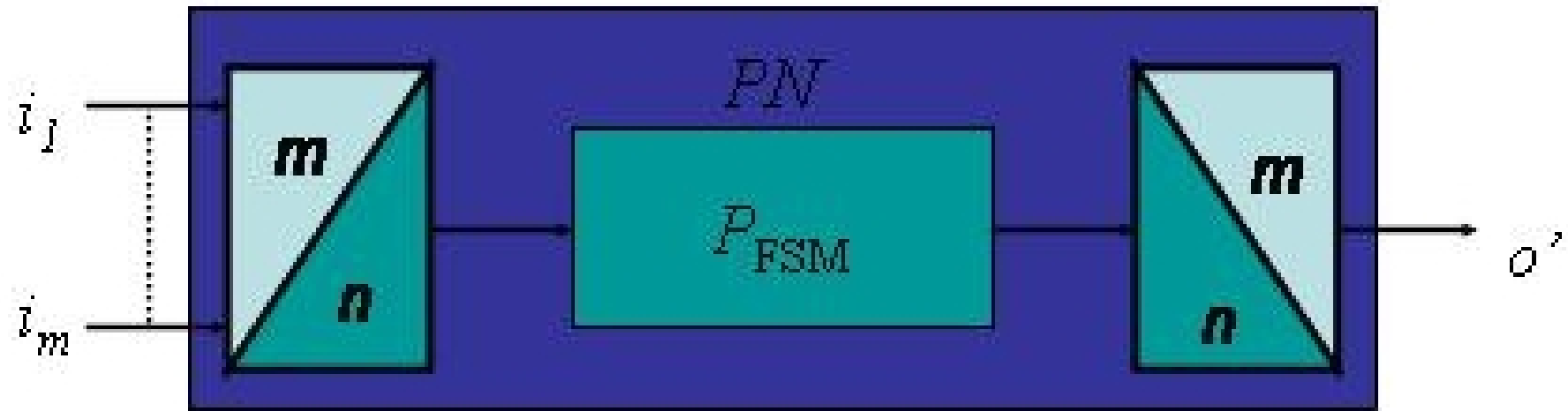
*SerialClockDomain*



Parallel/Serial

Downsample

# Transformation Rules - Scheduling



**Parallel/Serial**

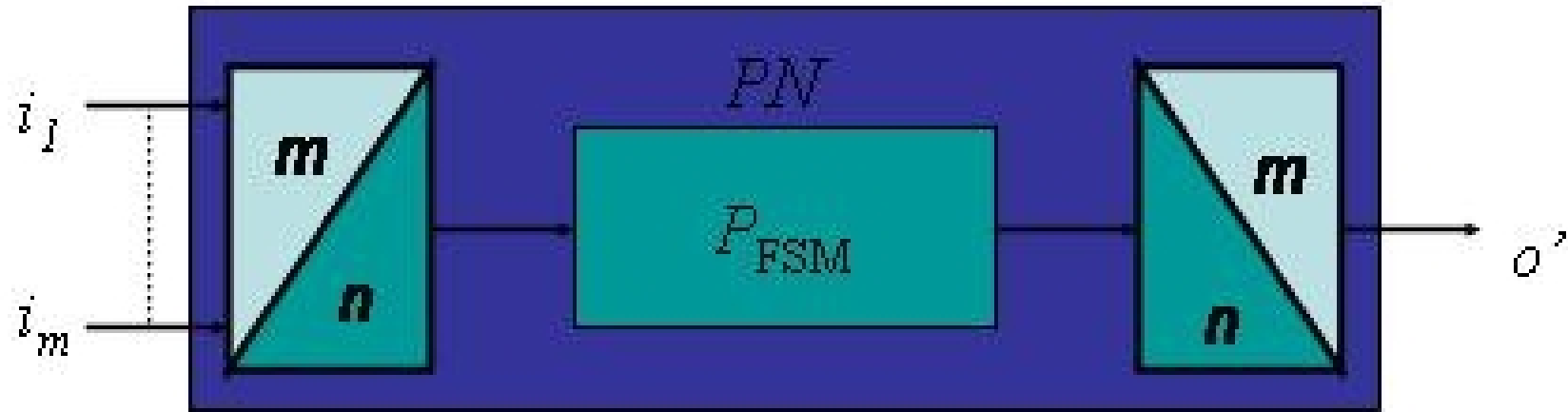
**Downsample**

$\neq$





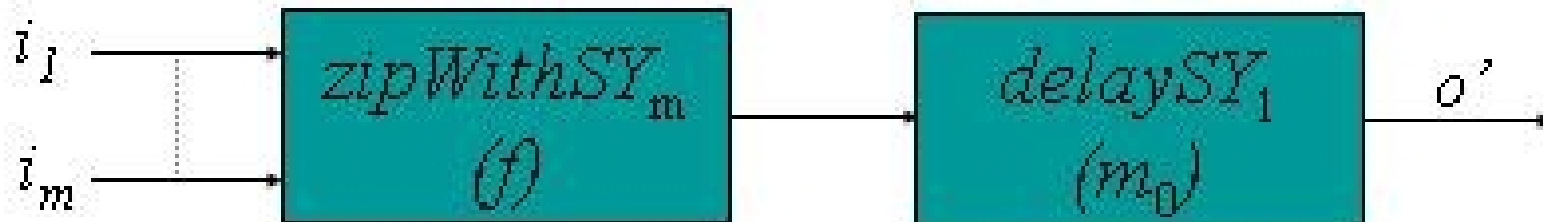
# Transformation Rules - Scheduling



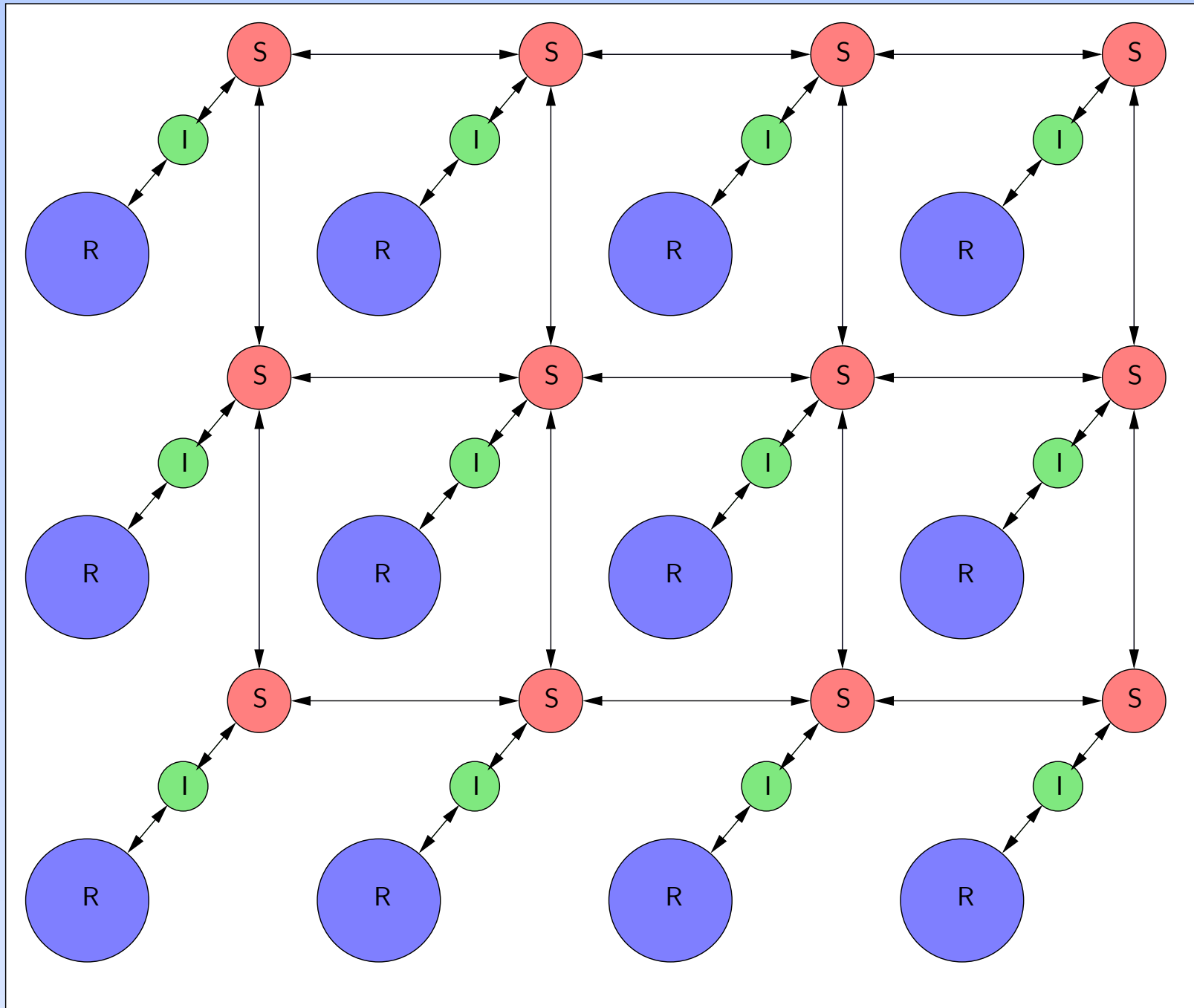
**Parallel/Serial**

**Downsample**

**=**



# NoC Simulator Case Study



# ForSyDe Status

## Ideal System Model

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Stable modeling technique  
U-MoC, S-MoC, CS-MoC, DT-MoC  
ForSyDe library based on Haskell

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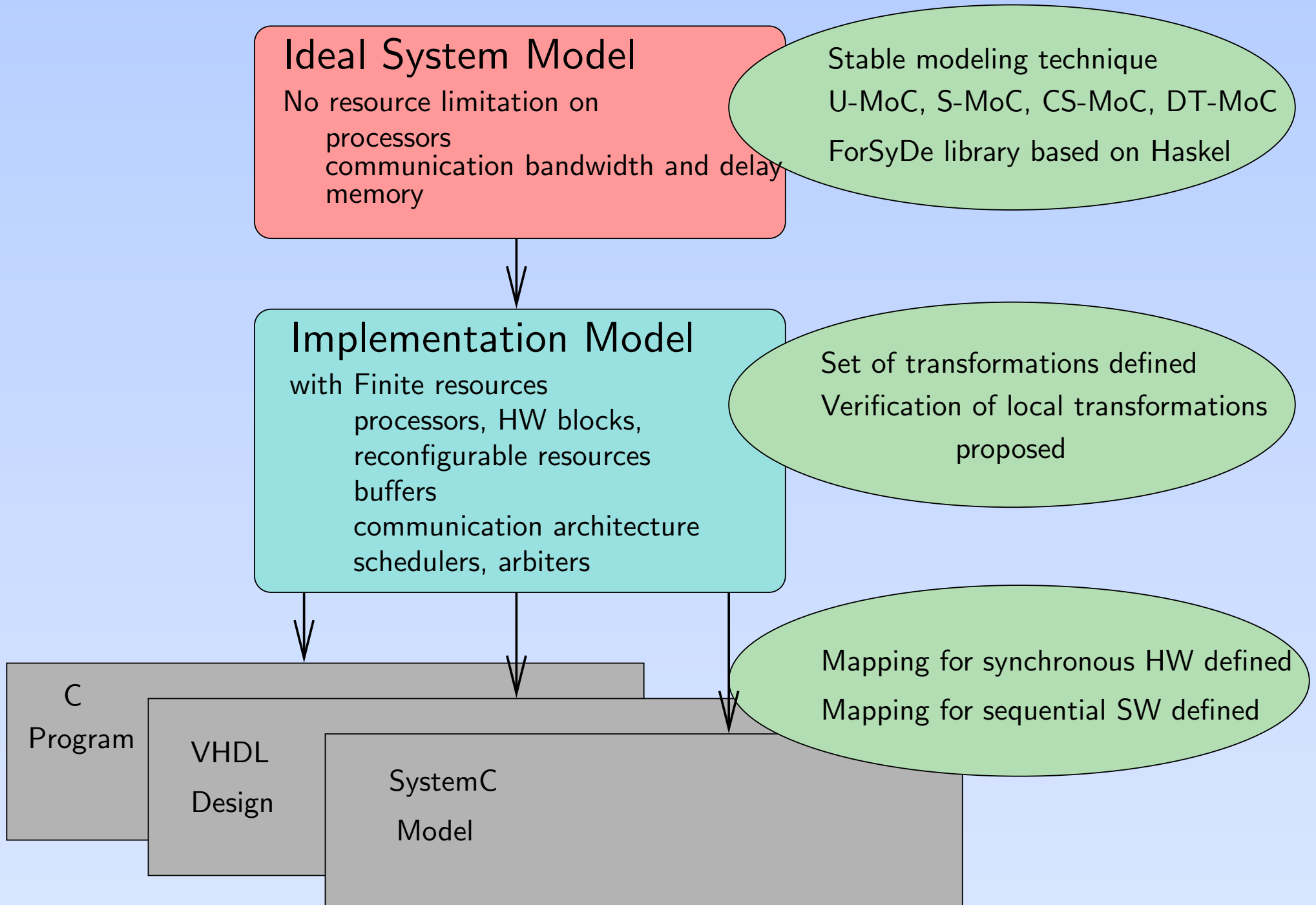
Set of transformations defined  
Verification of local transformations  
proposed

Mapping for synchronous HW defined  
Mapping for sequential SW defined

C  
Program

VHDL  
Design

SystemC  
Model



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## Ongoing work

Definition of a CT-MoC  
Modeling of non-functional properties  
Modeling of adaptive resources  
GME based tool support for transformations  
Communication refinement method

Mapping for synchronous HW defined  
Mapping for sequential SW defined

C  
Program