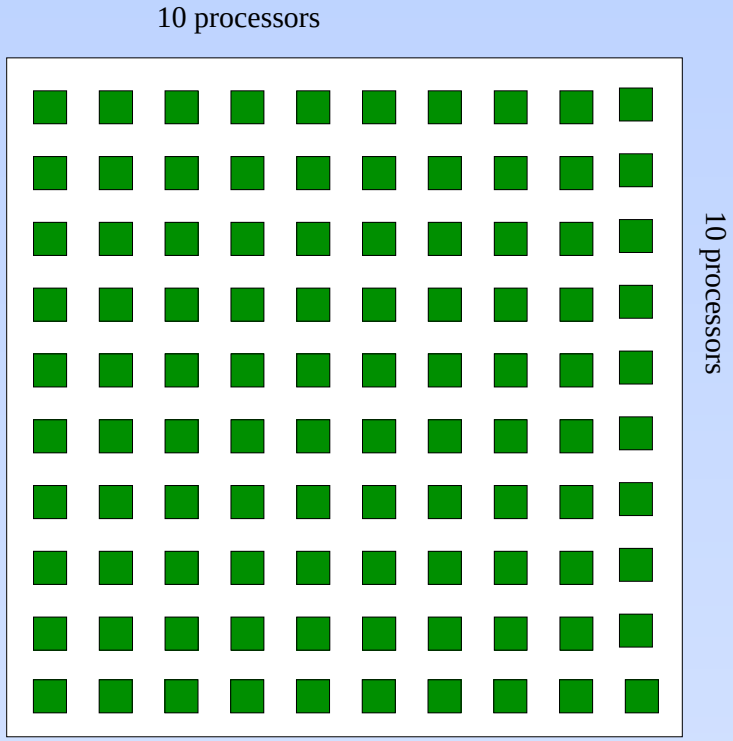
Networks on Chip



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Royal Institute of Technology, Stockholm

April 2003

Overview

Introduction

Topology and Structure

Protocol Stack

The Network Layer and the Switch

Data Protection

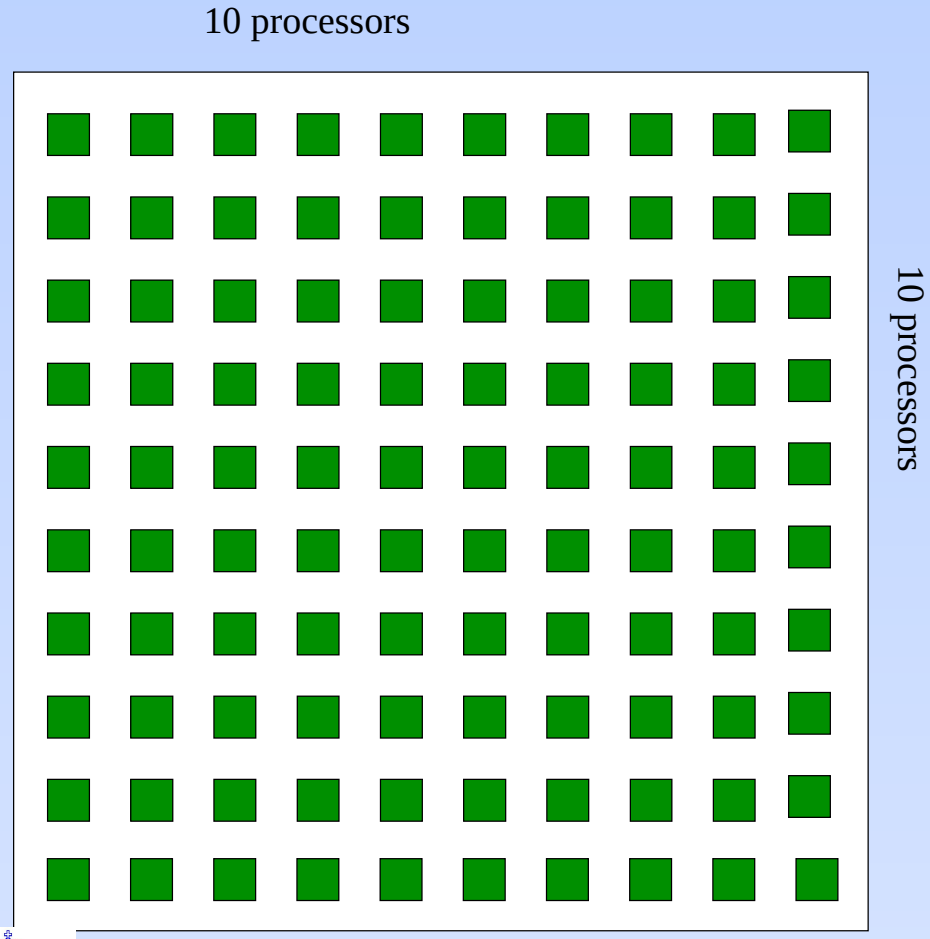
The Session Layer

NoC Simulator

Performance Evaluation

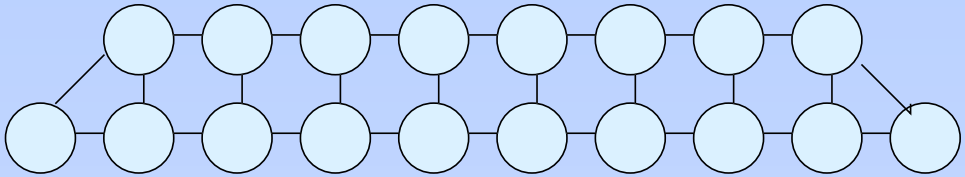
Emulation Environment

The Challenge

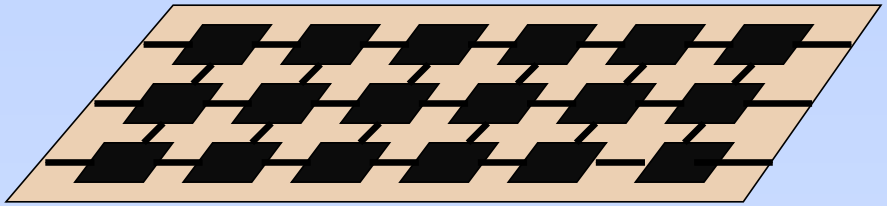


# Gates	# Processors	Year
6 M	4	2000
24 M	16	2003
96 M	64	2006
384 M	256	2009

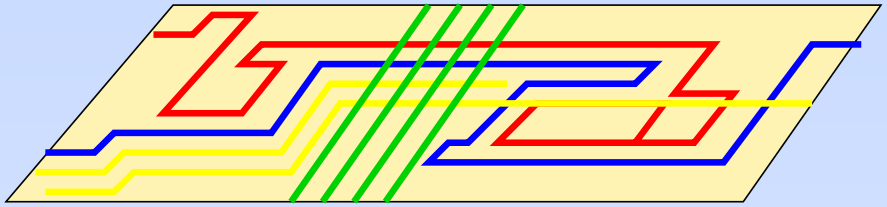
Functions, Architecture, and Physics



Concurrent processes



Large number of resoucres



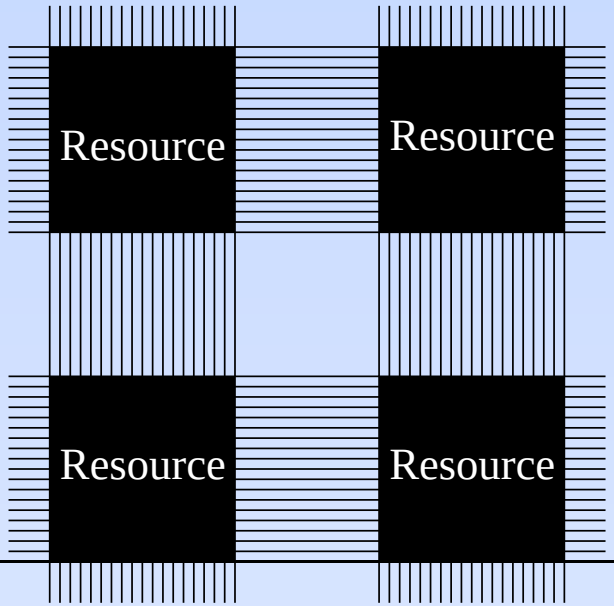
Physical issues

Motivation

- A systematic approach to on-chip communication is a necessaity;
- General platform for a variety of applications;
- Flexibility by means of selection of resources and communication services;
- Reuse of design and verification of communication services, architecture and implementation;
- Reuse of resources and features (system functionality + resource implementation);
- Better controllable physical properties;

Challenge Areas: Physical Issues

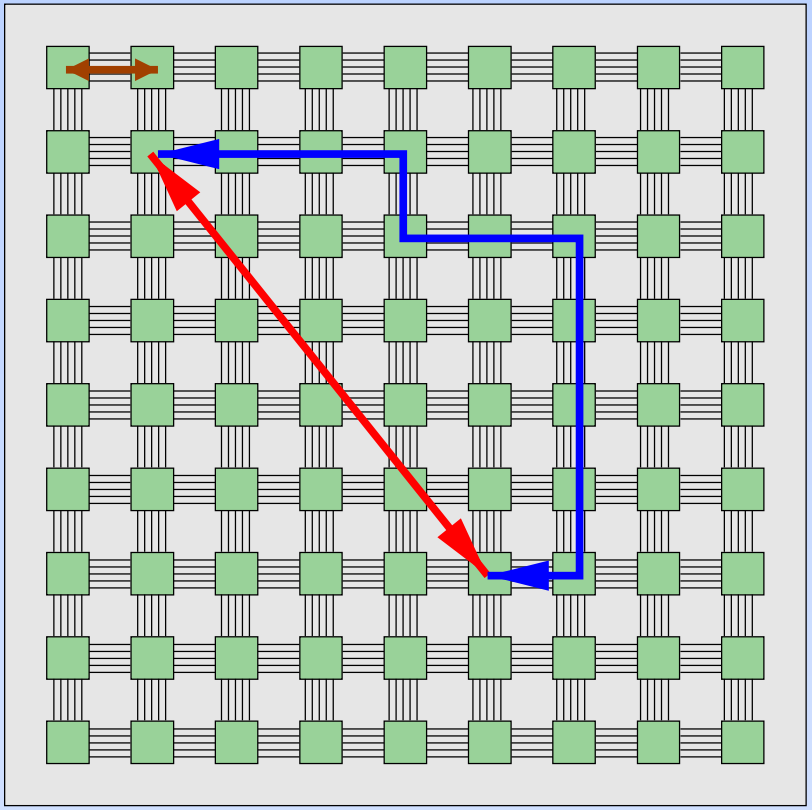
- Deep submicron effects, noise, signal integrity
- Interconnect
- Power consumption, power delivery
- Clock distribution
- Memory integration (50-80% of the chip)



Scenario:

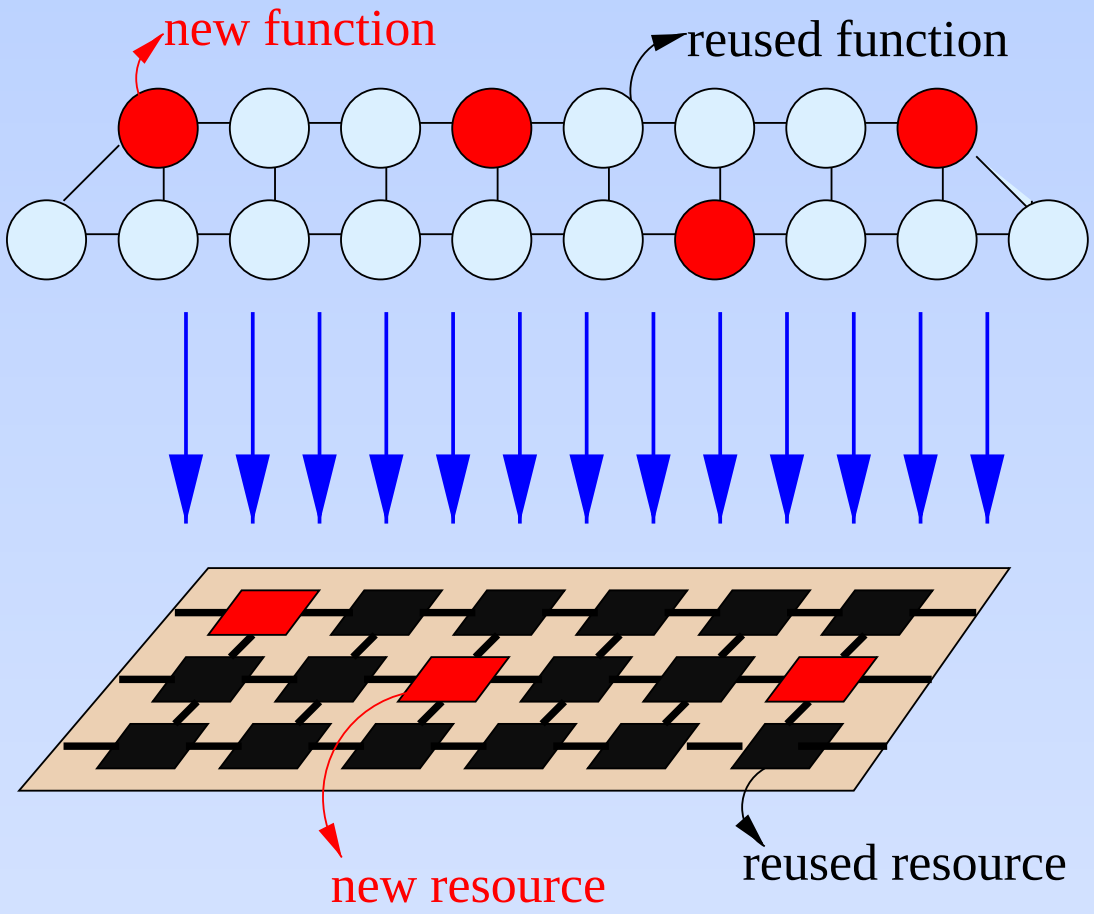
- 60 nm CMOS
- 22×22 mm Chip size
- 2×2 mm resource size
- 300 nm minumum wire pitch
- 6600 wires between two resources on each metal layer

Challenge Areas: Architecture



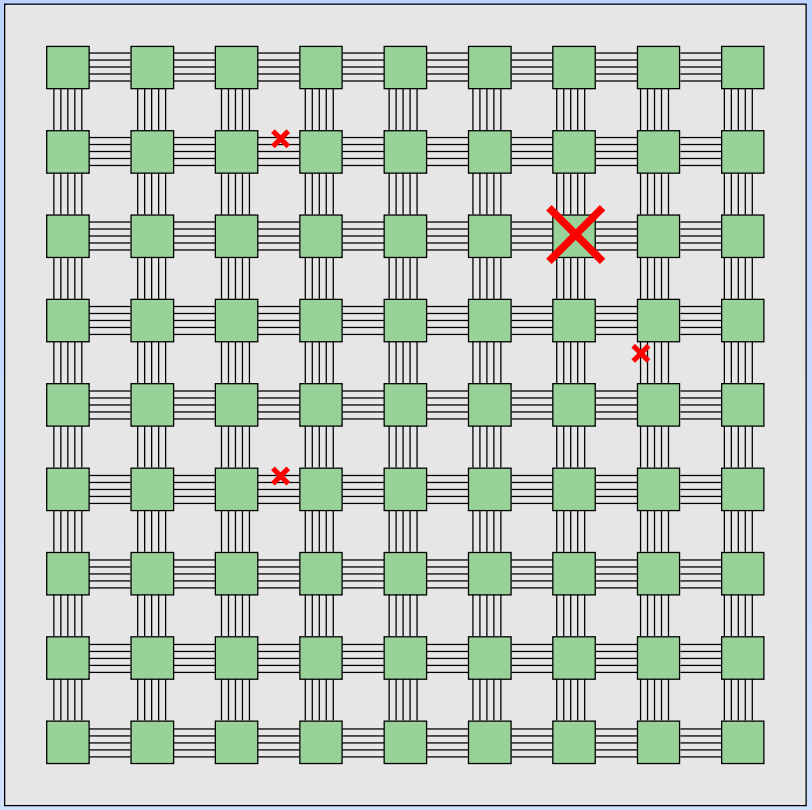
- Communication infra-structure
  - ⋆ Physical layer
  - ⋆ Data link layer
  - ⋆ Network layer
  - ⋆ Transport layer
- Type and size of resources (Micro processor, DSP, memory, FPGA, etc.)
- Resource usage

Challenge Areas: Methodology



- Specification techniques of concurrent activities
- Performance analysis
- Reuse and Integration of both functions and components

Challenge Areas: Run Time Services



- Monitoring
- Fault-tolerance,
- Diagnostics
- Fault recovery
- Dynamic resource management

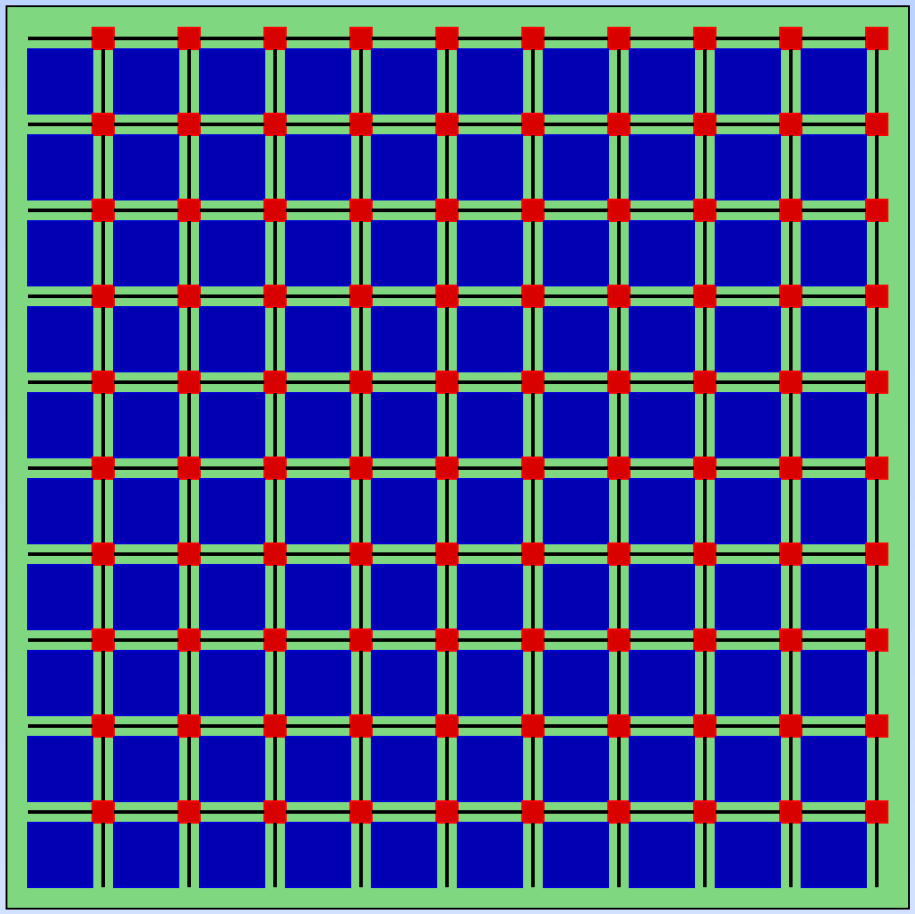
Challenge Areas: Configurability

A sensible trade-off between efficiency and generality is critical.

- Configurability of communication resources from the data link to the application layer
- Configurability of resources (processors, DSPs, FPGAs, etc.)
- When and who?
  - ⋆ Design-time configuration: Platform ⇒ Pruduct
  - ⋆ Static product configuration: Once for a product
  - ⋆ Dynamic reconfiguration: Programming of the product

Overview

Topology: Mesh



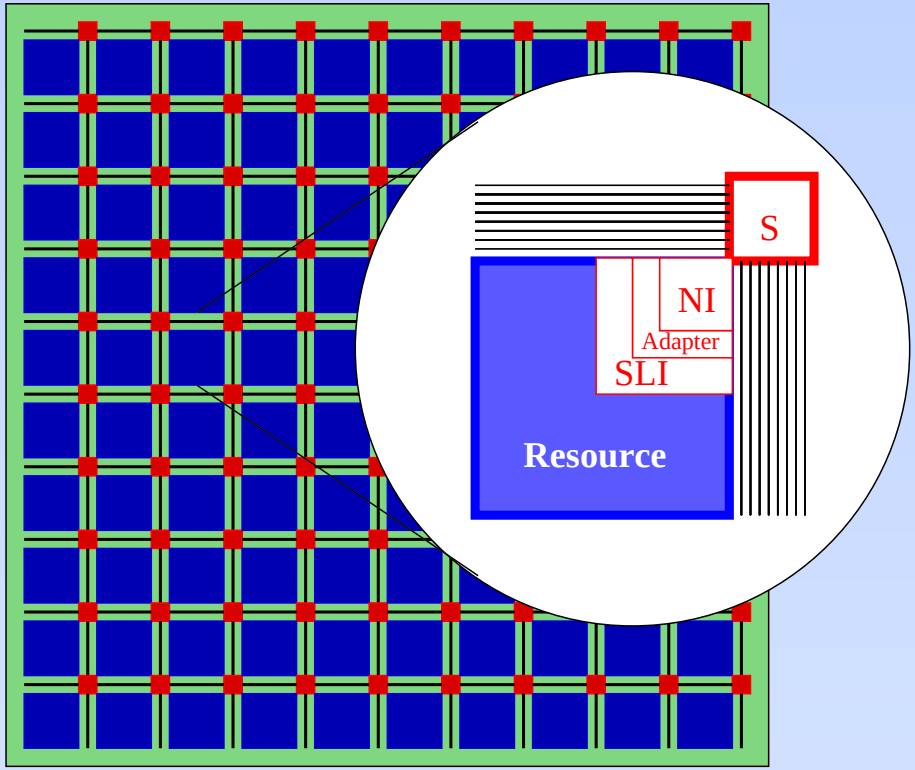
Characteristics:

- Resource-to-switch ratio: 1
- A switch is connected to 4 switches and 1 resource
- A resource is connected to 1 switch
- Max number of hops grows with $2n$

Motivation:

- Regularity of layout; predictable electrical properties
- Expected localitry of traffic

The Node in a Mesh



NI: Network Interface:

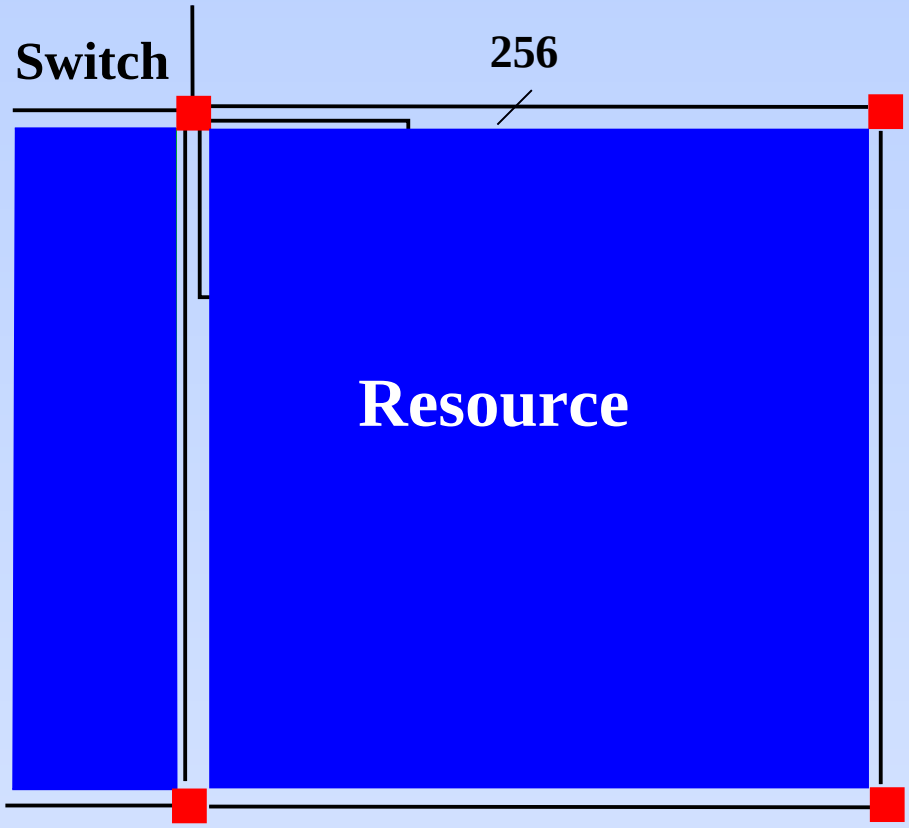
- Compulsory
- HW
- Implements the network layer protocol

Adapter: Resource specific interface circuit;

SLI: Session Layer Interface:

- Optional
- Hardware and/or software
- Implements the session layer protocol

Node Geometry

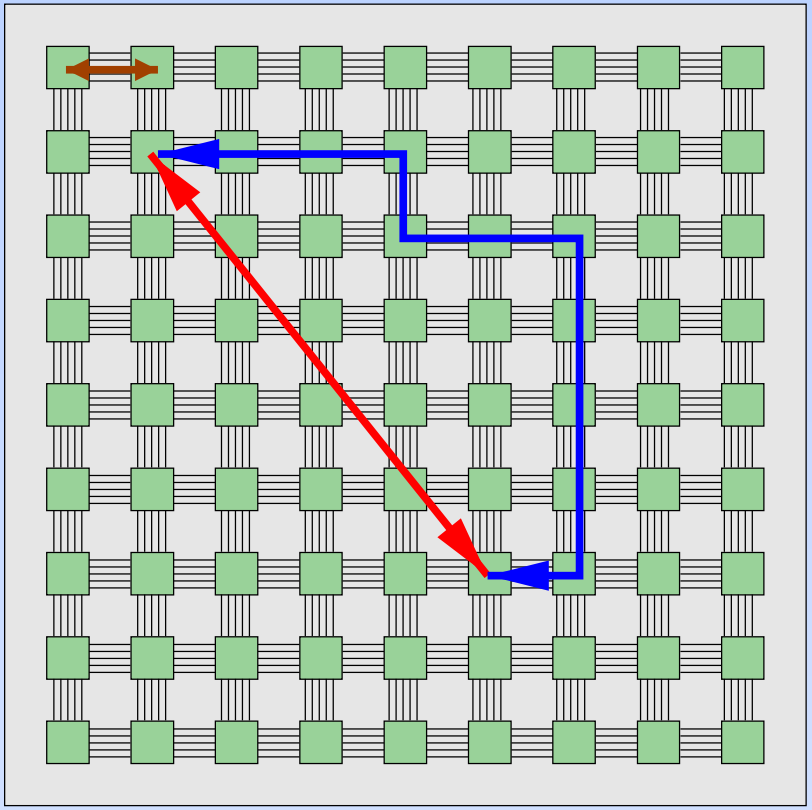


Scenario:

- $60nm$ CMOS
- $22mm \times 22mm$ chip size
- $300nm$ minimal wire pitch
- $2mm \times 2mm$ resource
- $100\mu m \times 100\mu m$ switch
- switch-to-switch connection: 256 wires
- switch-to-resource connection: 256 wires

Overview

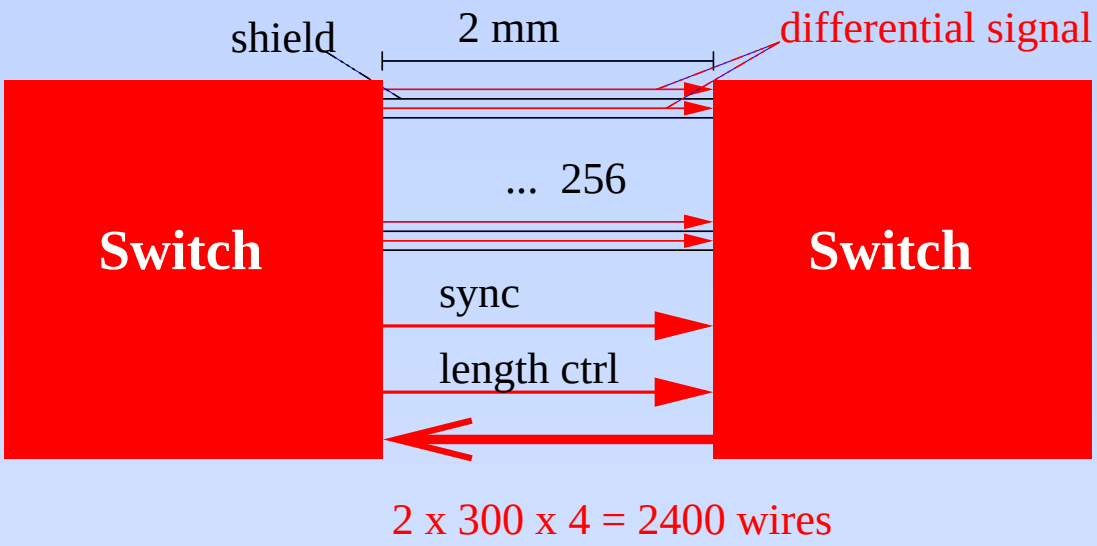
Communication is Key



Communication Layers:

- Physical layer: switch-to-switch and switch-to-resource
- Data link layer: switch-to-switch and switch-to-resource
- Network layer: resource-to-resource
- Session layer: process-to-process
- Application layer: application-to-application

Physical Layer



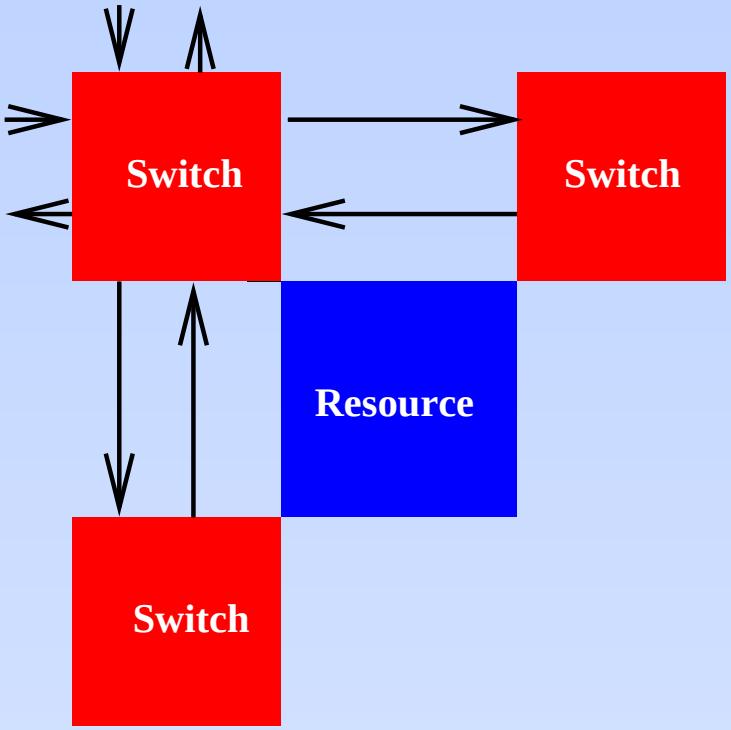
Parameters:

- Physical distance
- Number of lines
- Activity control
- Buffers and pipelining

Nostrum status:

- 128 data lines in each direction
- No pipelining
- On/off control for power saving

Data Link Layer



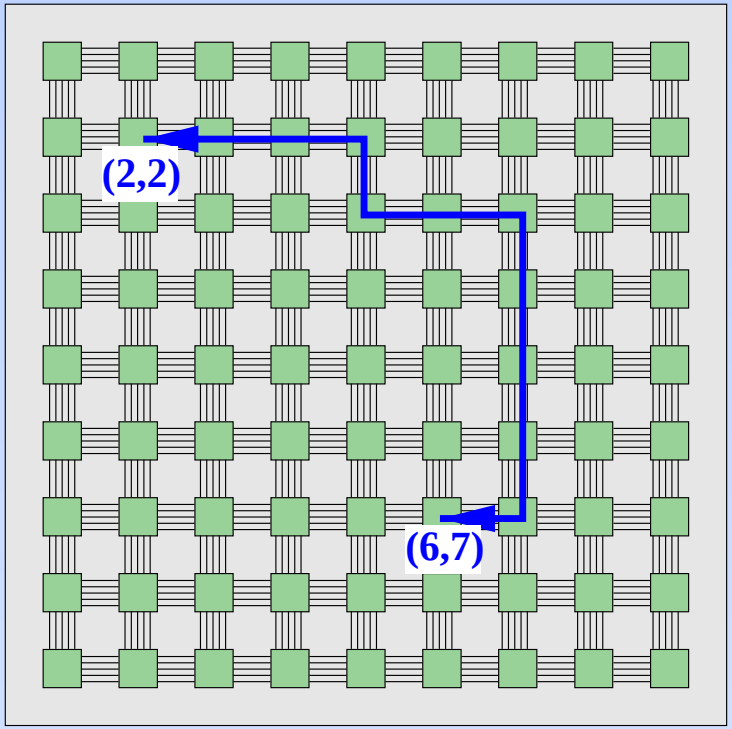
Parameters:

- Line frequency versus switch frequency
- Buffering
- Error correction
- Power optimization encoding

Nostrum status:

- Physical packet = data link packet
- Physical clock = data link clock
- Single packet input buffer
- Error correction
- On/off activity control

Network Layer



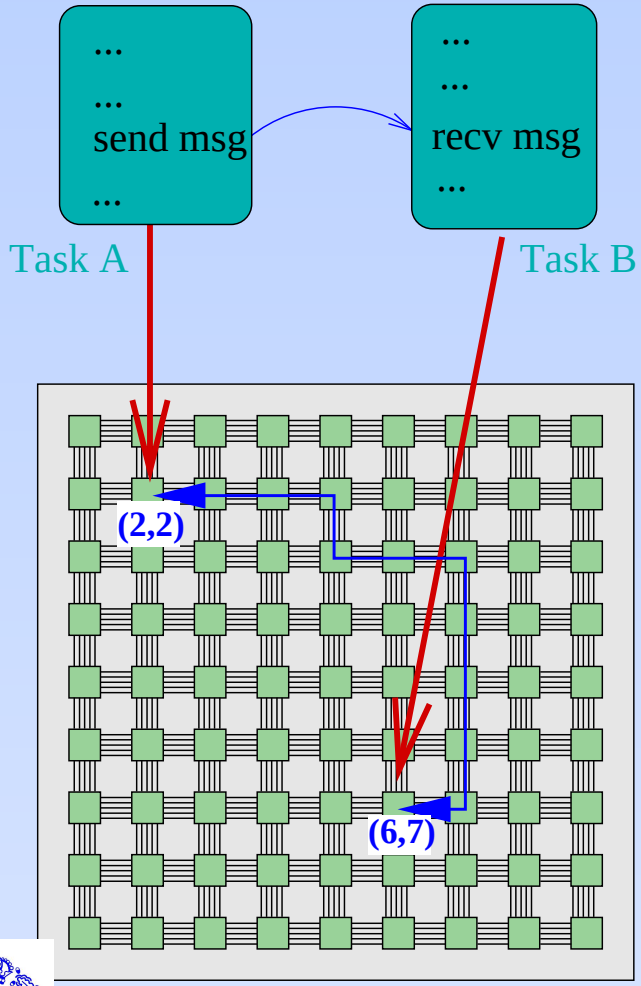
Parameters:

- Link layer cell size vs. network layer packet size
- Network address scheme
- Routing algorithm
- Priority classes
- Error correction

Nostrum status:

- Link layer packet = network layer packet
- Relative x-y addresses
- Deflective routing with no buffers and no routing tables
- Virtual circuits with guaranteed bandwidth and delays
- No error protection

Session Layer



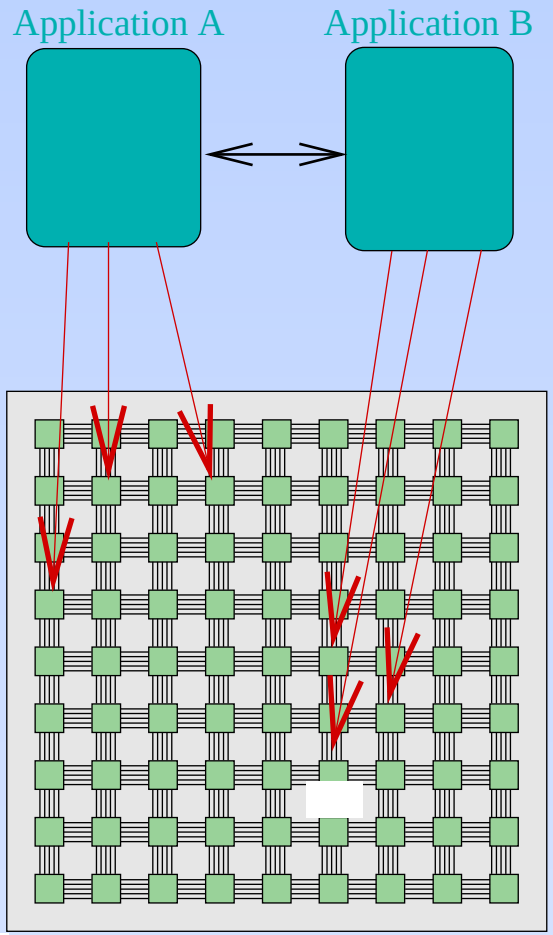
Parameters:

- Task level communication primitivs
- Message passing
- Shared memory based communication
- Synchronization
- Error correction

Nostrum status:

- Set of communication primitivs defined
- Both message passing and shared memory
- User controlled synchronization
- Optional end-to-end data protection

Application Layers



Application specific communication services;
E.g. the NoC operating system could use:

- Task/resource database access protocol
- Task migration protocol

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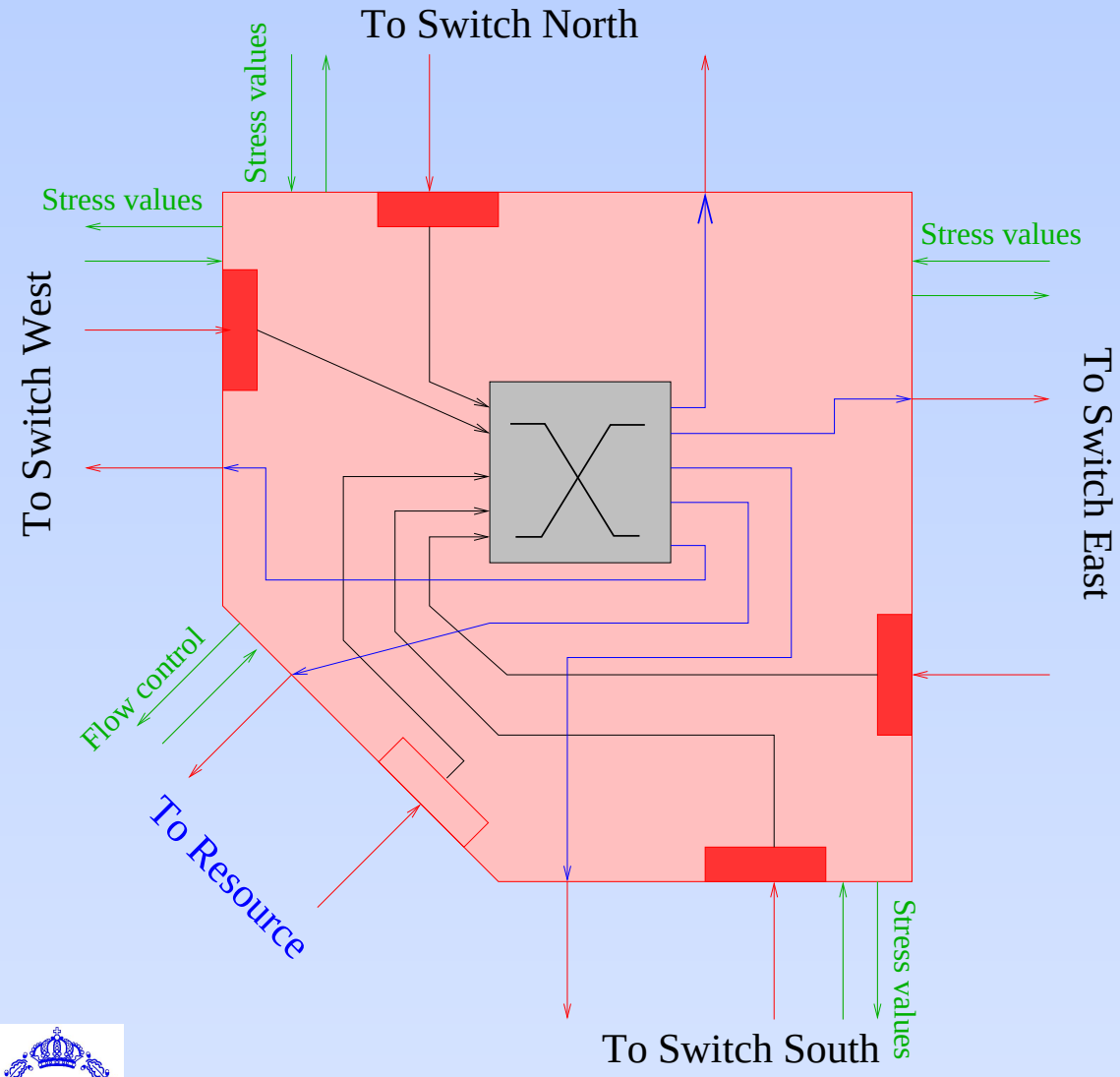
The Network Layer

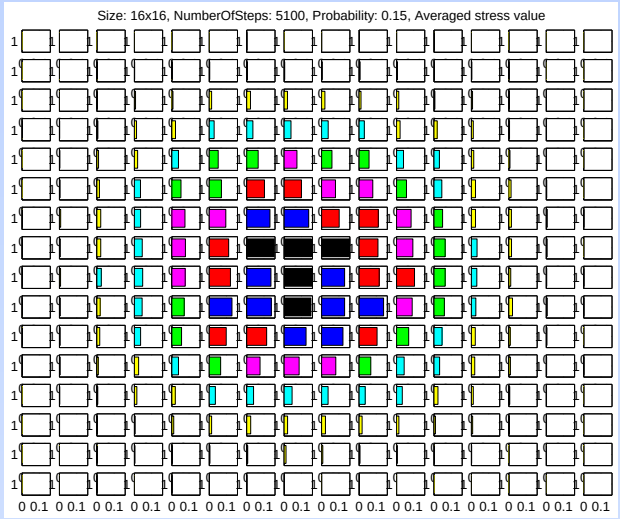
- Packet switched best effort service
  - ⋆ Packets are guaranteed to arrive
  - ⋆ Packet payload may be protected (4 levels of protection)
  - ⋆ Load dependable delay in the network
  - ⋆ Load dependable delay at the network access point
- Virtual circuit service
  - ⋆ Guaranteed bandwidth
  - ⋆ Guaranteed maximum delay
  - ⋆ Multicast circuits
  - ⋆ Based on packet switching service

The Bufferless Switch

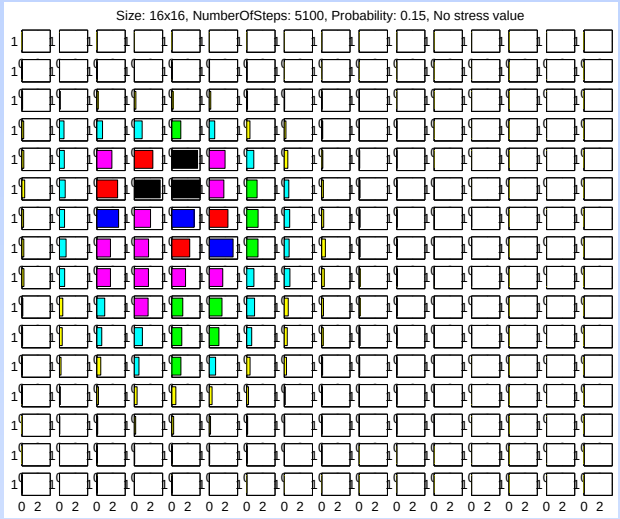


- \+ No buffers
- \+ No routing table
- \+ Small area
- \+ Short delay
- \+ Low power consumption
- – Non-shortest path
- – Header overhead due to destination address

Stress Value Effect on Buffer Sizes and Delays

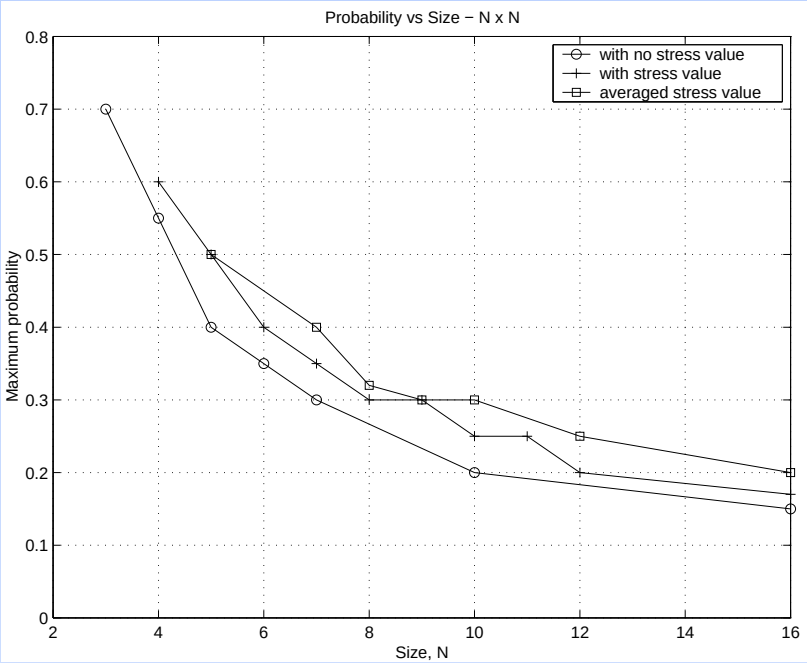


Largest average buffer size: 3.2



Largest average buffer size: 0.1

Stress Value Effect on Maximum Load



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Data Protection

- Two level protection: Link layer and session layer
- Data link layer protection:
  - ⋆ SEC-DED header protection (16/26 bits)
  - ⋆ Four levels of payload protection:
    - ∗ Maximum bandwidth - no protection (102/102 bits)
    - ∗ Guaranteed integrity - DED protection (90/102 bits)
    - ∗ Minimum latency - SEC protection (90/102 bits)
    - ∗ High reliability - SEC-DED protection (81/102 bits)
- Session layer:
  - ⋆ Normal mode 1-4: Selection of link layer protection
  - ⋆ Reliability mode: packet acknowledgment/retransmission

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Session Layer Communication

- Message passing communication:
  - ⋆ `open/listen/accept/bind` primitives to open a channel
  - ⋆ `send/receive` to communicate
  - ⋆ `close` to tear down the channel
  - ⋆ blocking/non-blocking send/receive
- Shared memory communication:
  - ⋆ allocation
  - ⋆ read/write
  - ⋆ free
  - ⋆ interruptable/non-interruptable
- VHDL,C and SystemC libraries under development

Overview

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NoC Simulator

- Implemented in SystemC;
- Organized along protocol layers;
- Configurable topology;
- Open resource interface

Simulator Features

- Topology exploration considering a subset of protocol layers;
- Experiments with switch and network layer design;
- Experiments with resources and work load models;
- Monitoring network activities;
- Collecting and visualizing network statistics;
- Script interpreter for controlling simulation;

Overview

Performance Evaluation

- Required performance metrics:
  - ⋆ Utilisation, load
  - ⋆ Bandwidth, latency, jitter
  - ⋆ Loss behaviour
  - ⋆ Power and energy consumption
  - ⋆ Reliability and fault tolerance
- Different metrics at different layers:
  - ⋆ Link level for raw performance;
  - ⋆ Network level for end-to-end behaviour;
  - ⋆ Application level for measuring application level performance;
- Well designed benchmarks to measure all this;

Summary of Nostrum Status

- Nostrum defines a 2 D mesh topology;
- Protocol stack for link layer, network layer and session layer;
- Packet switched and virtual circuit communication services;
- Buffer-less, loss-less switch with no routing tables;
- 2 level data protection scheme;
- Session layer communciation primitives;
- Flexible NoC Simulator;
- Plan for performance assessmen;

Further information: www.imit.kth.se/info/FOFU/NOC/