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# Self-selection pseudo-circuit: a clever crossbar pre-allocation

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**Abstract:** This paper proposes self-selection pseudo-circuit (SP), a simple and effective approach to increase switch connection reusing rate and improve the network performance. It especially suits the network in which the performance is dominated by the number of hops. In SP scheme, multiple switch connections are allowed to be reserved for one inport, and the flit can reuse the partial switch connection(s) based on the routing information. For the evaluation with the traces from Splash-2, SP reduces the interconnection latency by up to 21.6% (16.9% average) with 16-core CMP configuration, and 22.2% (19.5 on average) with 64-core CMP configuration. Evaluated with synthetic traffic, the proposed scheme decreases the latency up to 19% (16% average).

**Keywords:** interconnection architecture, Network-on-Chip

**Classification:** Integrated circuits

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## 1 Introduction

In chip multiprocessors (CMPs), communication latency is sensitive to the number of hops that the packet is routed. To further enhance the network performance, recent research reduces the per-hop latency using speculation, look-ahead computation, etc. [1, 2, 3], which complicates the router significantly. Matsutani et al. proposed predictions router which predicts the outport to be used by the next packet, and if the prediction hits, the next packet can be transferred without waiting for the routing computation and switch arbitration [4]. Pseudo-circuit is proposed to reduce the per-hop latency by reusing the switch connection of departing packet [5]. However, in pseudo-circuit scheme, the condition of reusing is tight, only with the same inport, virtual channel and outport as the departing packet can the packet reuse the connection. Packet Chaining, relaxes this condition that allows any virtual channels in the same inport to reusing the connection, which improves the reusability considerably [6].

We observe that temporal locality of every application has a common characteristic, that some particular inport is frequently used and the outport may be changed alternately. In this paper, we introduce self-selection pseudo-circuit, which allows multiple switch connections to be reserved for one inport, to further improve the reusability and enhance the performance. To avoid mis-transferring the flit to undesired outport, the routing information is used to determine whether the flit passes through or not.

## 2 Detailed description

### 2.1 Router architecture and variant of pseudo-circuit

We use XHINoC (Extendable Hierarchical and Irregular Network-on-Chip) as our router [7, 8, 9]. XHINoC adopts a method named wormhole cut-through


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switching, which allows the wormhole messages to be interleaved at the flit-level in the same buffer and share the communication links. Each flit of the same packet can be routed correctly by using a local ID, which is unique in each communication channel. Since the virtual channel is removed from the router, switch allocation (SA) is reduced to one level, which is between inport and outport. A round robin arbiter is integrated in each outport to select the inport in a fair way. The condition of pseudo-circuit reusing in our router is simplified as follows: the same inport and the same outport, where the virtual channel matching is removed. Thus, the probability of connection reuse is improved. This variant of pseudo-circuit is named VP in this paper. XHINoC has four stage pipelines: Buffer Write, Buffer Read + Route Compute, Switch Arbitration (SA) and Switch/Link Traversal (ST/LT), and VP tries reusing the switch connection to bypass SA.

### 2.2 Self-selection pseudo-circuit

Self-selection pseudo-circuit (SP) allows multiple arbiters to keep the switch connections to the same inport, and a waiting packet can select desired outport(s) according to routing information, which we call it self-selection. A new waiting packet is suitable for reusing the switch connection if (a) it's outport belongs to the reserved connection(s), (b) there is a free buffer to hold one flit in the downstream router.

In our scheme, pseudo-circuit comparator logic (PCL) is used to determine whether a flit can bypass SA. It contains a register ($P$) to record arbitration history, and a comparator to compare the routing information of selected flit. In this paper, N, E, W, S indicate the directions of the ports, and L is the port attached to a IP. Fig. 1 (a) gives the partial structure of the PCL in inport L, which matches the pseudo-circuit between inport L and outport N. When arbiter N gives a grant to inport L, the N bit of $P$ in inport L is set to 1 while the N bits of $P$ in other inports (W, S and E) are cleared to 0 simultaneously. Register O contains the routing information of the flit. The N bits of $P$ and $O$ are viewed as the input, and the output signal are *hit* and *req*. If signal *hit* is 1, the pseudo-circuit can be used, and if signal *req* is equal to 1, it needs SA.

One important issue of reserving multiple connections to single inport is to avoid mis-transferring the flit to an undesired outport. To overcome this problem, we use routing information to select the passage strategy. As can been seen in Fig. 1 (b), the control wire connected to the N bit of $O$ will allow the flit to pass through the multiplexer and be forwarded to the downstream router directly by the reserved connection. The N bit in $O$ will be cleared to 0 in next cycle. When the outport of the follow flit is not N, all-0-bit will be output to outport N by the reserved connection.

The additional delay caused by pseudo-circuit comparison (PC) is negligible compared to pipeline period [5], and can be fit into ST/LT and SA when they are not the critical path. If PC succeeds, the current stage is PC+ST/LT, and the flit goes through a three-stage pipeline. Otherwise, the current stage is PC+SA, and a four-stage pipeline is needed. There is no


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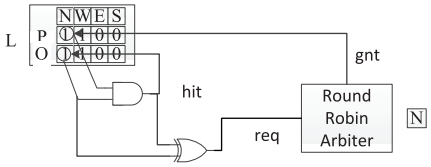
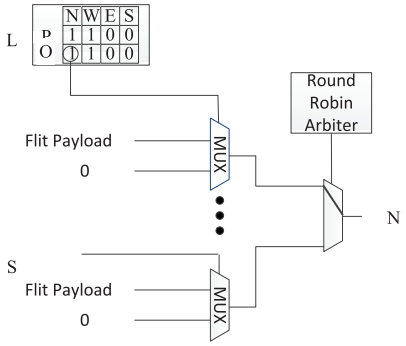
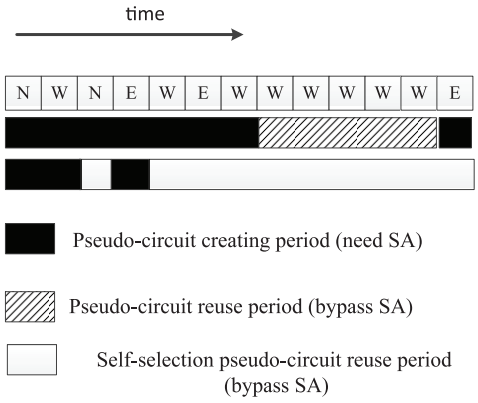



(a) The pseudo-circuit comparator logic




(b) The pseudo-circuit self-selection logic




(c) An Example from Real Application Trace

**Fig. 1.** Proposed self-selection pseudo-circuit scheme

performance overhead when PC fails.

Fig. 1 (c) gives an example showing the efficiency of SP. There are 13 sequential outport requests from individual flits at the same inport, which we observe from the trace of real workload (barnes). During this period, none of the outports labeled in time slots is requested by other inport. The slots colored black denotes that the corresponding flits need SA, and will create a new pseudo-circuit. The slash slot indicates the flit can reuse the pseudo-circuit, where the white slot denotes that of our scheme. Pseudo-circuit [5] switches the connection when outport is changed, and only 5 flits can reuse switch connection. However, if SP is adopted, the number of reuse is 10. Hence, SP extends the pseudo-circuit by allowing multiple ports to reserve the connections for one inport, which improves the reusability.

Compared with pseudo-circuit [5], the hardware and power overhead increased by self-selection pseudo-circuit is negligible. All the overhead is just some multiplexers which combine all-0-bit and flit.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## 3 Experiment methodology

We developed a cycle-accurate network simulator based on XHINoC. Deterministic dimension-order routing is adopted for its simplicity and efficiency. We evaluate the SP using the trace extracted from Splash-2 [10], and the synthetic workload traffic is also included. We report the result of XHINoC without any optimization as the baseline. For the reason of virtual-channelless router being adopted, the result of VP is also presented. VP should have higher pseudo-circuit reusability than that in wormhole router with virtual channels [5].

In the experiment of real applications, we extract the traces from Splash-2 by Simics [11]. Our CMP configuration has 16/64 processors, of which each has a L1 I/D Cache (64 KB, 4 way set-associative) and L2 Cache (256 KB, 8 way set-associative). Each processor is attached to one router in a $4 \times 4$/$8 \times 8$ mesh, and 8 memory controllers are distributed at the borderline of the mesh. The data width is set as 32 B.

In the evaluation of the synthetic workload, we use uniform, bit complement, bit reverse, bit rotation, shuffle, transpose and tornado traffic patterns [12]. Due to space limitation, we only report the latency result at 0.05 flit/node/cycle. None of the patterns reaches saturation at this rate. The network size is extended to $8 \times 8$ mesh.

## 4 Evaluation

### 4.1 Performance with traces

Fig. 2 (a) depicts the overall pseudo-circuit reusability in all Splash-2 applications (parallel phase only) with 16-core CMP configuration. Pseudo-circuit reusability is defined as the percentage of flits reusing pseudo-circuit [5]. It is expected that more performance improvement benefits from the higher reusability. The reusability of variant of pseudo-circuit (VP) is up to 71% (54% on average), while SP offers up to 86.5% (67% on average) reusability. Fig. 2 (b) shows the latency with the baseline, VP and SP under the application workload. The latency of the baseline is normalized as 1. VP offers up to 17.8% (13.6%) latency reduction, and SP up to 21.6% (16.9% on average) latency reduction. Fig. 2 (c) gives the reusability with 64-core CMP configuration. The reusability of VP is up to 71.8% (57.2% on average), and that of SP is up to 88.6% (77.4% on average). In this case, VP gains a latency reduction 14.4% on average, while SP reduces latency 19.5% on average.

### 4.2 Performance with synthetic traffic

The evaluation under the synthetic workload is also considered. Fig. 3 (a) shows the reusability in the synthetic traffic. The reusability of VP is up to 41% (36% on average), and SP offers up to 76% (63% on average) reusability. We can observe that the difference between VP and SP is more aggressive than that in the trace experiments. Especially for the bit complement, the reusability of SP is improved about 214% compared with VP. The reason is the synthetic traffic has more communication-pairs (node to node) existing


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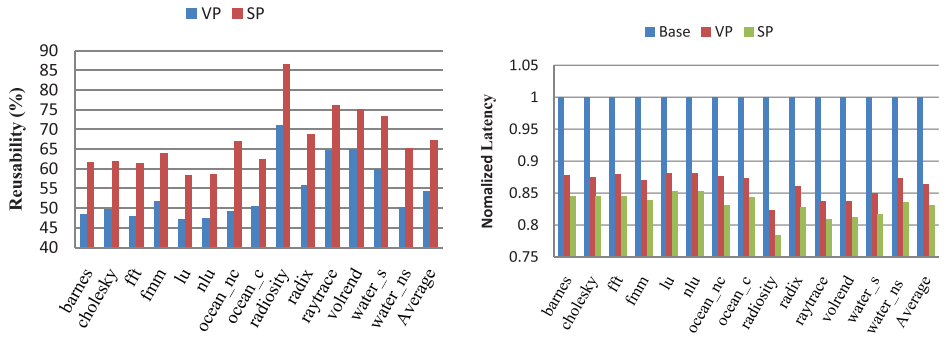
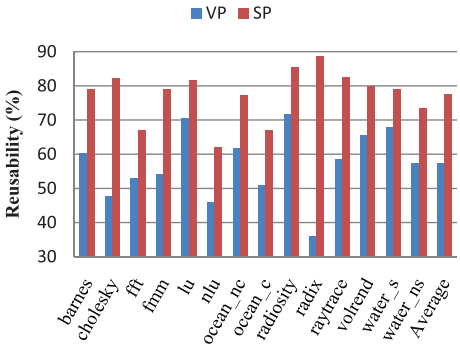


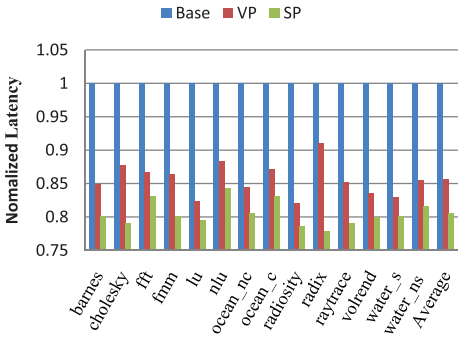

(a) Reusability under the Traces with 16-core CMP




(b) Latency Reduction under the Traces with 16-core CMP

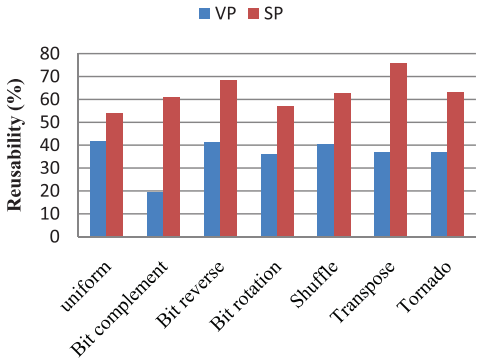



(c) Reusability under the Traces with 64-core CMP

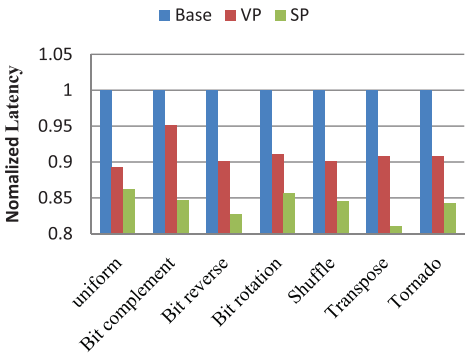



(d) Latency Reduction under the Traces with 64-core CMP

**Fig. 2.** Performance with traces




(a) Reusability




(b) Latency Reduction

**Fig. 3.** Performance with synthetic traffic

concurrently, which may change the connection frequently. VP has limited ability to adapt to this situation, and SP is highly adaptable to it.

Fig. 3 (b) depicts the latency under the synthetic traffic. We evaluate the performance under different injection rate at the flit level. Under the low-load traffic, the latency reductions of VP with uniform, transpose and bit complement traffic patterns are 10.7%, 9.2% and 4.9%. Overall, this result is consistent with paper [5]. The subtle difference comes from that our $8 \times 8$ mesh gives more communication-pairs than $4 \times 4$ in [5], which may vary the connections in the router more frequently. When the load increases, the reusability will decrease when more virtual channels are used which leads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mis-matching of virtual channels. However, the reusability of VP and SP are stable when the injection rate increases, for the reason of removing of virtual channel. VP gives the latency reduction up to 10.7% (9% average), while SP offers up to 19% (16% average).

## 5 Conclusion

SP extends the pseudo-circuit by allowing multiple connections to be reserved for one inport, which efficiently utilizes temporal locality in a compatible way. The evaluation result shows that the proposed scheme improves the performance significantly. To evaluate SP with other topologies and routing algorithms is our future work.

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