Low-Power and Error Coding for Network-on-Chip Traffic

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Abstract:

The goals of this paper are to explore adaptability of low-power coding techniques, and estimate error coding overheads for Network-on-Chip (NoC) bus interconnections. Our simulations show that bus-invert encoding and partial bus invert encoding are not efficient due to their large overheads. On the other hand, implementation of error protection codes in the switch has only a small influence on both power consumption and time delay.

1. Introduction

The common way to implement on-chip communication is using shared buses. However, this approach has limited scalability that is why it will not be able to satisfy communication requirements of future platforms. One way to overcome these limitations is to separate computation from communication. The computational resources of a system will communicate by global interconnection architecture, called Network-on-Chip (NoC). In [5] the Nostrum architecture was proposed which is based on a regular $m \times n$ mesh of the Resources (R). A resource can be any IP block like processor, DSP, FPGA, any kind of memory, etc. Every resource connects to the network by means of a Resource Network Interface (RNI). The network interconnections are bidirectional with 128 lines width to the one direction. The network is based on packet switching. The Switch (S) is the fundamental building block inside the NoC backbone, it distributes all traffic through the network. The switches themselves are bufferless and use hot-potato routing [5].

Power consumption will be a key limiting factor in future NoCs. In the NoCs, the power is dissipated on two components: 1) the switches, located in the cross-points of network and 2) the interconnect wires. These wires consume significant part (up to 50% [3]) of the energy in an integrated circuit, and this part is only expected to grow in future. For the NoC, this parameter becomes even more critical in consequence of long distance on-chip interconnect network.

As technology scales towards deep submicron, on-chip interconnects become more sensitive to noise sources such as power supply noise, crosstalk, radiation induced effects, that are likely to reduce the reliability of data [11]. For the NoC, this problem becomes extremely significant. To increase reliability several solutions for data protection has been proposed [11], [7]. However, their overheads are still unexplored.

The paper is organized as follows: Section 2 discusses the related work, Section 3 presents examined configurations and describes frameworks of simulation performance and power estimation, Section 4 presents the setup for simulation experiments, Section 5 introduces experimental results and gives their analysis, and Section 6 concludes the paper.

2. Related work

Various methodologies for reduction of bus power consumption has been presented in literature ([10], [17], [9], and [15]) and successfully applied to on- and off-chip communication. Though, all these methods are well investigated and widely implemented, none of them has performed their feasibility study for NoCs. A need of this examination follows from the architectural and purpose differences between SoC buses and NoC communication backbone.

In [15] and [2] several issues are described concerning applicability and inapplicability of low-power bus encodings for deep sub-micron buses. Hence, it is the focus of the research to show adaptability of these methods for a new architecture for future integrated computer and telecommunication systems.

There are several works, describing methods to estimate power consumption both on combinational logics and interconnect wires. L. Benini *et al.* suggested the Bit Energy approach [16] to calculate power dissipation on switch fabrics in network routers. They used look-up table, pre-calculated from Synopsys Power Compiler simulation.

The error-control techniques for NoC architectures were investigated in [11] and [7]. In these papers, several Quality-of-Service schemes with different levels of data protection were presented. Four of them were implemented in System C in [7]. In the contents of current research, one of these schemes was implemented in VHDL. Its power consumption, time and area overheads were estimated with Synopsys Power Compiler.

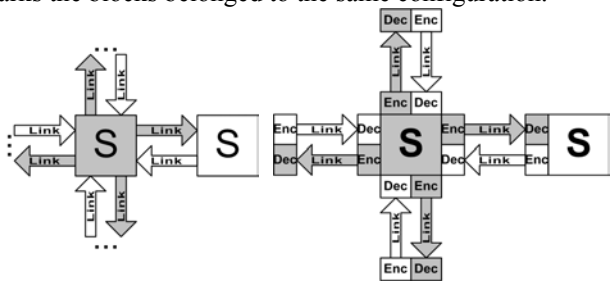
3. Methodology

a. Examined configurations of the NoC simulator

In order to investigate an influence of the low-power

technique the following basic configurations were chosen for further examination. The models of all design blocks are implemented in VHDL on the RTL level.

Configuration A. This is the baseline configuration which consists of the switch (S) and four adjacent network interconnection buses – Links (see Figure 1a) that communicate with the neighbor switches. The grey color marks the blocks belonged to the same configuration.



a) Configuration **b) Configurations B, C, and D**

Figure 1: Examined configurations.

Configuration B includes four low-power blocks type 1 by each side of the switch. They consist of the Encoder (Enc) and the Decoder (Dec) (see Figure 1b).

Configuration C is similar to the previous configuration but here we use low-power block type 2. In all other respects the functionality is the same. (see Figure 1b).

Configuration D. In this configuration instead of the low-power block the error-control block is used which consists of Encoder (Enc) and Decoder (Dec) (see Figure 1b).

b. Dataflow simulation experiments

To measure and compare the power consumption of the NoC for different configurations, several models were involved in simulation process. All of them simulate functionality of different parts of the NoC.

The Resource Model and the Dataflow Analyzer were specially developed in the contents of current research and implemented in MatLab. They operate on the Network Layer.

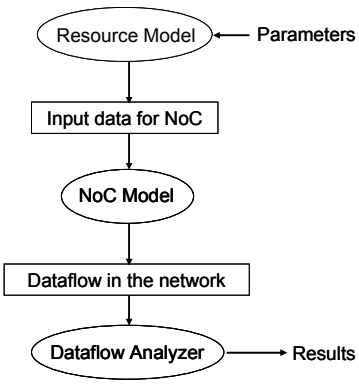


Figure 2: Simulation dataflow.

Figure 2 shows dataflow of simulation process which consists of three stages. During the first stage, according to the input parameters Resource Model generates data messages that are used as an input data for the NoC Model.

On the second stage, the NoC model performs dataflow simulation by sending prepared messages from their sources to the destinations and saves information about the data streams, transmitted through each interconnection bus in the output file (Dataflow in the network).

During the last stage, the Dataflow Analyzer estimates network load and switching activity using the information, saved in the previous stage. The output results are presented both in numerical and visualized graphical formats.

c. Power estimation

The following framework was used to estimate the power dissipation of the implemented design blocks. In the first stage, the highest possible frequency of the design is estimated by the Synopsys. Second, the power consumptions of the design blocks are estimated by the Synopsys. Next, all values of the clock frequency and power are scaled to the 65 nm technology. Then, the power consumption of the network is calculated for the 65 nm technology, using the following equation:

$$P_{Net} = \tfrac{1}{2}\alpha C_{Net} V_{DD}^2 f \,, \quad (1)$$

where C_{Net} is interconnection wires capacitance; α is the bit switching activity in the network. Its value is estimated during the dataflow simulation experiments. V_{DD} is the power supply voltage and f is the clock frequency.

The overall power consumption equals to the sum of power consumed in the design blocks and network interconnections scaled from the 180 nm to the 65 nm technology. The figures and scaling methodology was taken from International Technology Roadmap for Semiconductors [8].

Since the several different techniques with various operating frequencies will be examined, it is essential to normalize their values to the lowest one in order to have the same throughput.

Furthermore, as the frequencies will be scaled to one value the supply voltage should be scaled as well in order to obtain fair results.

4. Experimental setup

There are two types of parameters used in simulation experiments: input and output parameters. The input parameters are used to handle simulation process. The following table presents their chosen values:

TABLE 1: EXPERIMENTAL SETUP.

Simulation parameters	Values							
Simulation type	Pseudo-real traffic (MP3)				Random traffic			
Mesh size	5x5		8x8		5x5		8x8	
Packetizaton	1	10	1	10	1	10	1	10
Emission probability	5-7 values such that Network load hits the range 20-70%							

There are two simulation types: pseudo real traffic and random traffic. In pseudo real simulation a compressed MP3 data is used as a payload of the data packet. Thus,

we can simulate a communication functionality of the NoC that operates with the compressed audio, video or other information. For the random traffic, payload has totally random data. Performed experiments show that the behavior of the pseudo-real traffic is very close to the random. That is why the following simulations will be proceeded with the random traffic.

Mesh size of the NoC backbone determines the number of switches used in current simulation. The experiments were performed with up to 8×8 meshes. Packetization is the number of packets, required to transmit the whole message from the resource. Emission probability is the probability that the resource will start the transition process in the current clock cycle. The simulations show that after 1000 clock cycles the results become quite stable. Therefore this value was chosen as a simulation time.

The output parameters are estimated during the simulation and are used as output data for further development. There are two of them:

1) Network load
2) Data switching activity

Network load is estimated for each clock cycle and defined as $L_{Net} = \frac{N}{N_{mux}}$, where N is number of packets, available in the network in the current clock cycle and N_{mux} is maximum possible number of packets: $N_{mux} = 4 \times m \times n$.

Data switching activity shows the ratio between number of switched bits and whole available number of bits. This parameter is estimated as average for the whole network and all cycles.

In order to find the most suitable low-power coding technique a lot of different schemes were studied. There are various types of bus-invert coding, code-book based coding, Gray code, working-zone coding, etc. The bus-invert coding was considered as the most appropriate according to the input parameters, namely: 1) it is optimal for compressed or random data [17]; 2) it does not require large memory for the dictionary (as the code-book based schemes need). Thus, the low-power block type 1 implements the bus-invert coding technique for the payload of the packet. And the low-power block type 2 implements partial bus-invert coding technique, which splits the payload into two parts and encode them separately.

The error-control block was implemented with Single Error Correction (SEC), and Double Error Detection (DED) for the packet header, and DED for the payload as described in [7].

5. Results and analysis

One of the main results of the performed simulation experiments is a distribution of switching activity through the data packet. In order to implement an efficient low-power technique we should know the packet fields that have the primary impact on the total switching activity.

Consider the network size 5×5, packetization 1, emission probability 0.4, network load 43.5%, total switching activity of the packet 18.2% and random traffic. Table 2 presents the part of total switching activity accounted to each packet field.

TABLE 2: SWITCHING ACTIVITY (SA) DISTRIBUTION.

	Addr.	Empty bit	Hop counter	Payload	Whole packet
Number of bits (Fraction, %)	16 (13.5%)	1 (0.8%)	6 (5.0%)	96 (80.7%)	119 (100%)
Average SA, %	11.0	39.5	10.1	21.4	18.2
Normalized SA, %	7.6	1.7	2.6	88.1	100

The majority of the packet switching activity (88%) is due to the payload, while it occupies only 80.7 % of number of bits. Thus, implementation of low-power techniques for the payload field will be most efficient.

As the main target of low-power coding was the reduction of the switching activity in the network interconnections, the following table presents the results.

TABLE 3: REDUCTION OF THE SWITCHING ACTIVITY IN 5X5 NETWORK.

Configuration	Average switching activity, %	Average reduction, %
A	20.8	-
B	19.6	5.8
C	19.0	8.7

Thus, the highest reduction that can be obtained after implementation of the Bus-Invert coding for the NoC interconnections is about 8.7%.

The minimal clock period of all design blocks scaled to 65 nm technology for different configurations is presented in Table 4.

TABLE 4: OPERATING CLOCK PERIODS OF THE DESIGN BLOCKS.

Conf.	Block	Clock period for the block, ns	Common clock period, ns
A	S	0.42 ns	0.42 ns (2.38 GHz)
	Link	0.08 ns	
B	S	0.42 ns	2.43 ns (0.412 GHz)
	Enc	2.43 ns	
	Dec	0.01 ns	
	Link	0.08 ns	
C	S	0.42 ns	1.28 ns (0.781 GHz)
	Enc	1.28 ns	
	Dec	0.01 ns	
	Link	0.08 ns	
D	S	0.42 ns	0.51 ns (1.96 GHz)
	Enc	0.04 ns	
	Dec	0.39 ns	
	Link	0.08 ns	

The values for the switch and network interconnection operating clock periods were presented in [6].

Since all four configurations work on different operating frequencies, their normalized frequency will be equal to 0.412 GHz. In order to obtain fair results, the supply voltages are scaled using the methodology described in Section 3.c.

Figure 3 and Table 5 presents the resulting power dis-

sipation of the four configurations.

TABLE 5: SWITCHING ACTIVITY AND POWER CONSUMPTION.

Conf.	Supply voltage, V	Block	Switching activity, %	Power consumption (50% of network load), mW
A	0.51	S	20.8	2.26
		Link (x 4)	20.8	281.23
			Total	*283.49*
B	0.90	S	20.8	7.03
		Enc (x 4)	20.8	7.98
		Dec (x 4)	19.6	0.86
		Link (x 4)	19.6	826.99
			Total	*842.86*
C	0.70	S	20.8	4.26
		Enc (x 4)	20.8	3.81
		Dec (x 4)	19.0	0.49
		Link (x 4)	19.0	484.28
			Total	*492.84*
D	0.53	S	20.8	2.44
		Enc (x 4)	20.8	3.17
		Dec (x 4)	20.8	1.49
		Link (x 4)	20.8	303.73
			Total	*310.83*

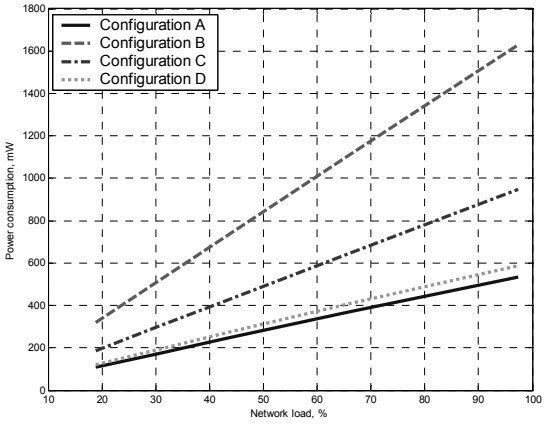


Figure 3: Configuration power consumption vs. network load

6. Conclusion

Thus, the simulation results show, that the payload switching activity has the main part in total packet switching activity and approximately equals to 88%. Therefore the implemented low-power techniques should target the payload. The switching activity is linearly dependent on network load. Implemented low-power techniques give at most 8.7% reduction of the switching activity in the network interconnection. Since in case of random data, that have uniformly distributed switching activity, Bus-Invert coding is optimal [13], other encoding techniques will perform worse. We have performed experiments with up to 8×8 meshes which confirm that our conclusions are independent of the mesh size.

Further estimations show that the time delay of the low-power block, leads to a fatal decrease in speed. Moreover, the reduction of power consumption as a result of the switching activity reduction does not compensate this overhead because the length of the interconnection buses is quite small. On the other hand, the implementation of error coding gives just about 9.6% overheads of power consumption and almost no time delays.

Thus, the performed experiments show that the examined low-power techniques are not suitable for the NoCs. The error protection mechanism [7] has some overheads but they are quite insignificant. Therefore, from power and delay point of view their implementations are feasible.

However, at present time work is underway on creating a guarantied bandwidth service for the NoC communication backbone using a virtual circuit. Such service will allow a large amount of information to be transferred through the fixed paths which could be quite long. In this case, an end-to-end low-power coding could achieve much more effective results.

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