TECHNISCHE UNIVERSITÄT WIEN
Vienna | Austria

Institut für Computertechnik
Institute of Computer Technology

Self Awareness and Resilience in CPS

Axel Jantsch

Testmethoden und Zuverlässigkeit von Schaltungen und Systemen

Freiburg, Germany, March 2018

Outline

1. Motivation
2. Concepts of Self-Awareness
3. Hardware Faults
   - Fault Types
   - On-line Diagnosis
   - Reliable NoC Design
   - Health Management
4. Self-Aware Monitoring
   - Context Aware Health Monitoring
   - Early Warning Score
5. Conclusions

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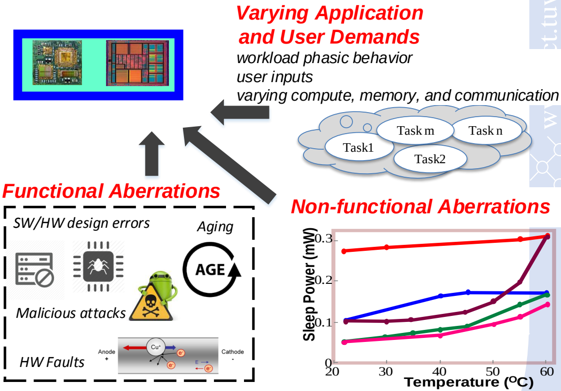
The Problem



Varying Application and User Demands

workload phasic behavior

user inputs

varying compute, memory, and communication

Functional Aberrations

SW/HW design errors

Aging

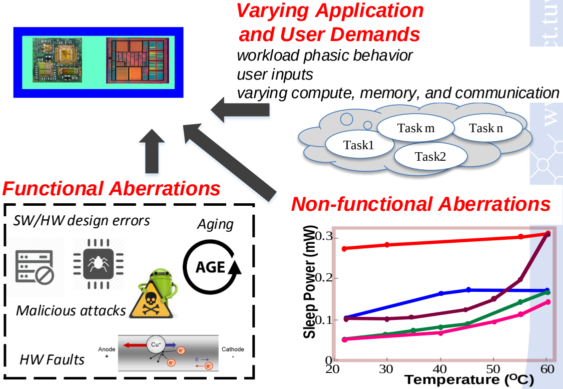
Malicious attacks

HW Faults

Non-functional Aberrations

The Problem

- Large number of resources



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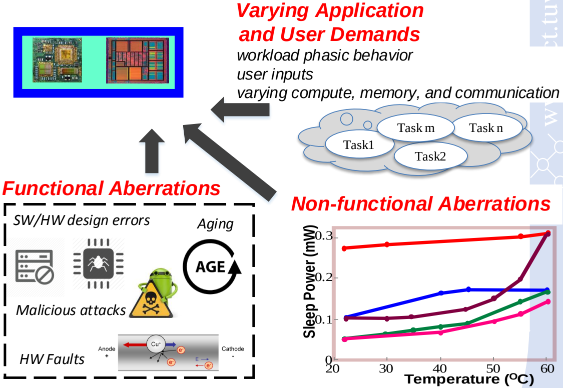

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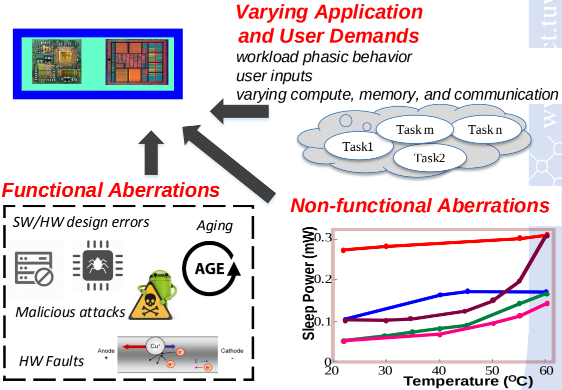
- Many tight constraints
- Varying application demands, both within and between applications;



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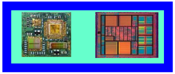
Non-functional Aberrations

The Problem

- Large number of resources
- Many tight constraints
- Varying application demands, both within and between applications;
- Functional Aberrations:
  - Design errors or omissions;
  - Malicious attacks;
  - Aging;
  - Soft errors;
- Non-functional Aberrations:
  - Performance;
  - Power consumption;



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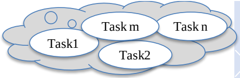
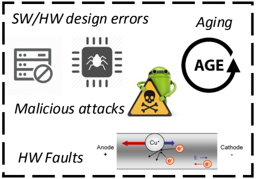
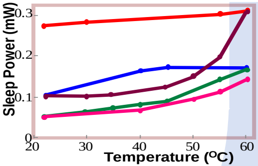


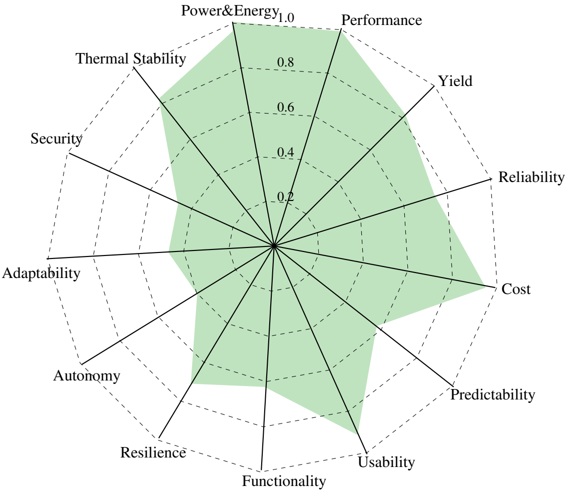
Functional Aberrations



Non-functional Aberrations

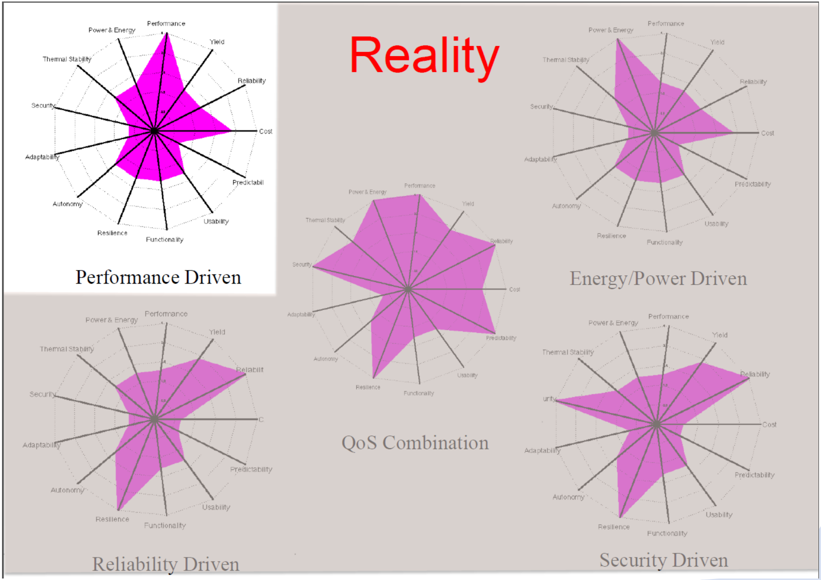


The SoC Radar



Santanu Sarma, Nikil Dutt, P. Gupta, A. Nicolau, and N. Venkatasubramanian. “On-Chip Self-Awareness Using Cyberphysical-Systems-On-Chip (CPSoC)”. . In: *Proceedings of the 12th International Conference on Hardware/Software Codesign and System Synthesis (CODES+ISSS)*. New Delhi, India, Oct. 2014

The SoC Radar



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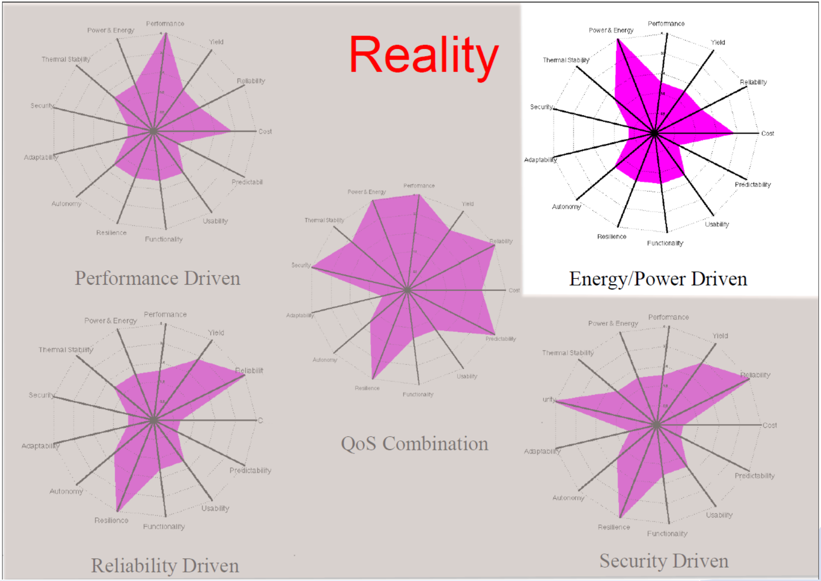

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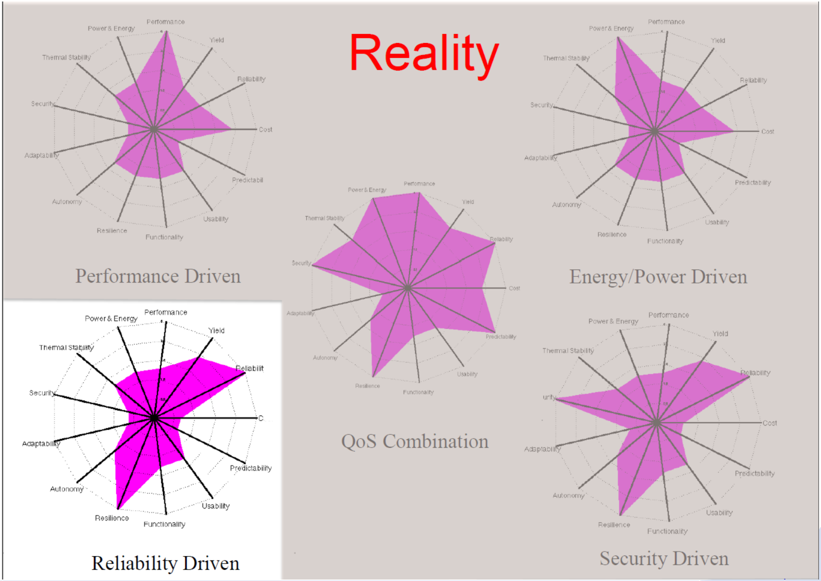


Reality

Performance Driven

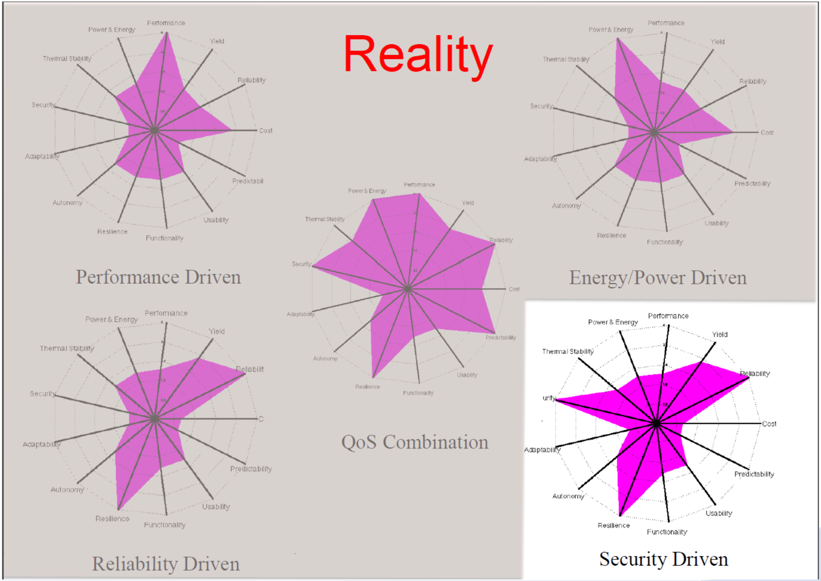
Energy/Power Driven

QoS Combination

Reliability Driven

Security Driven

The SoC Radar



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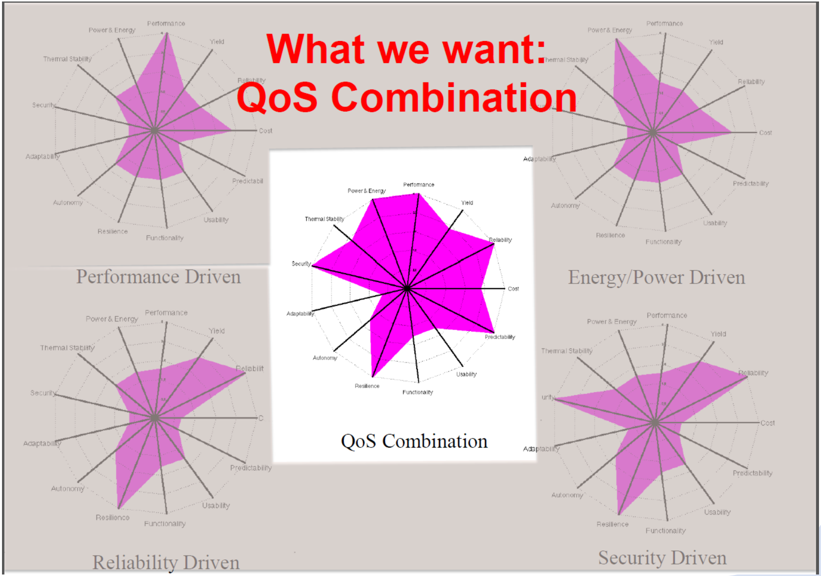

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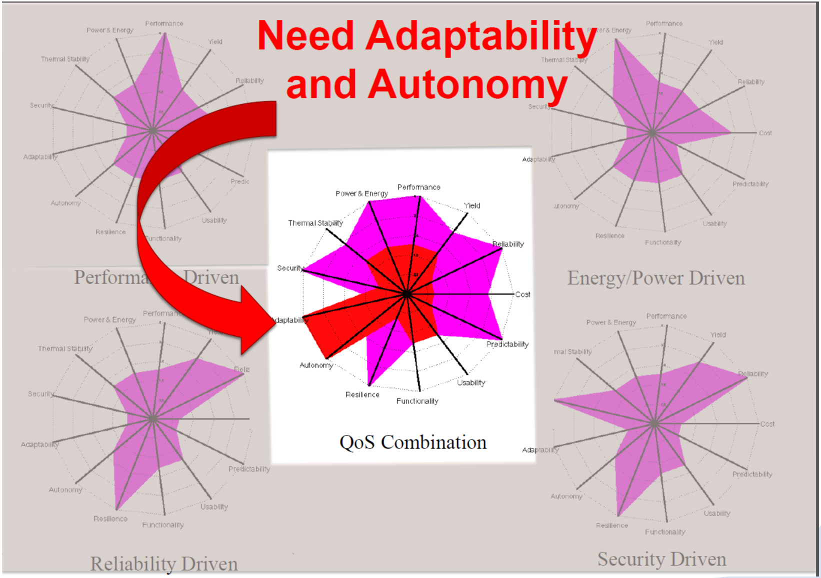

Need Adaptability and Autonomy

Performance Driven

Energy/Power Driven

QoS Combination

Reliability Driven

Security Driven

Self-Awareness

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Which Ingredients Lead to Awareness ?

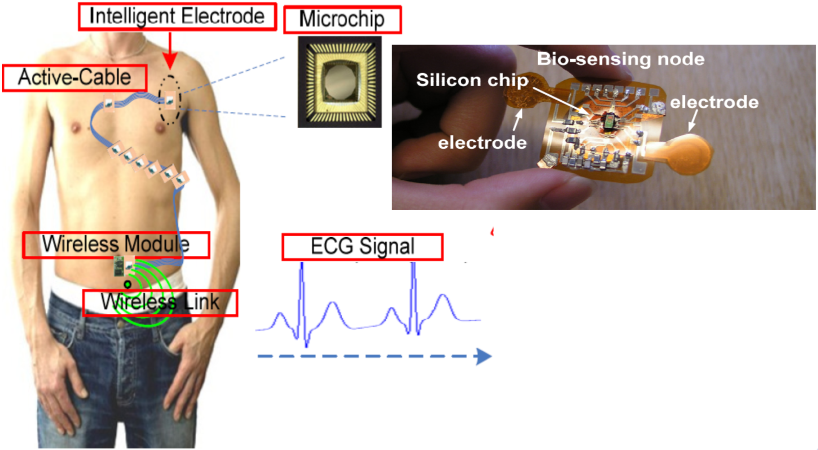
Johan Moreelses "Der Alchemist", 1630

Which Ingredients Lead to Awareness ?

- Data abstraction
- Disambiguation
- Desirability scale
- History
- Goals
- Attention
- Learning
- Introspection

Johan Moreelses “Der Alchemist”, 1630

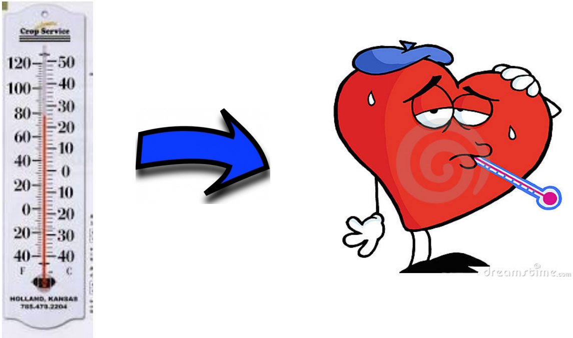
Awareness for Resource Constrained, Insect-like Gadgets



Courtesy of KTH

Abstractions and Models

Abstraction: Mapping of Measurements ⇒ Properties



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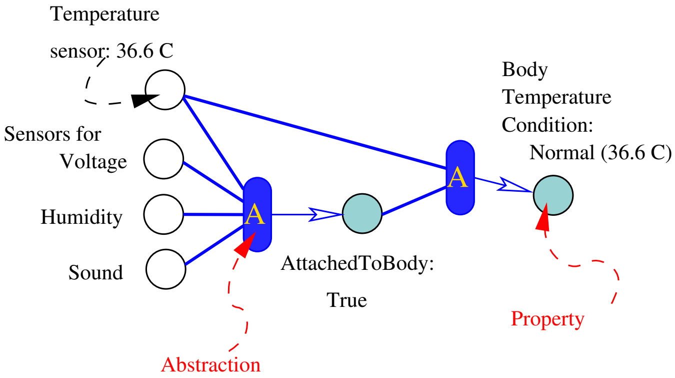


Temperature sensor: 36.6 C

Sensors for Voltage

Humidity

Sound

AttachedToBody: True

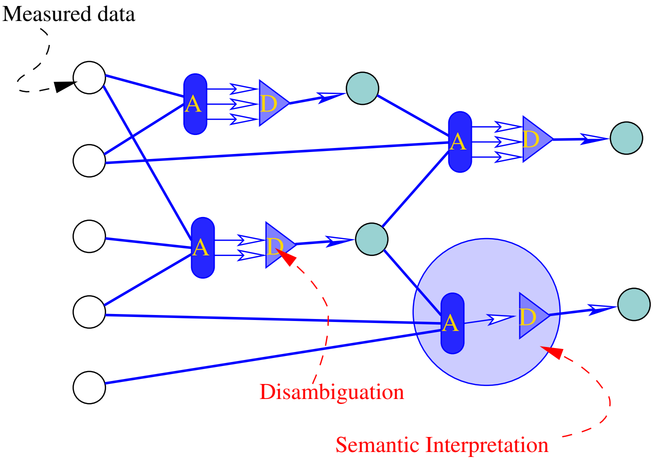
Body Temperature Condition: Normal (36.6 C)

Abstraction

Property

Disambiguation

Selection among several interpretations



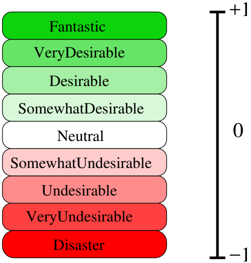
Measured data

Disambiguation

Semantic Interpretation

Desirability Scale

Desirability is the common, internal currency.

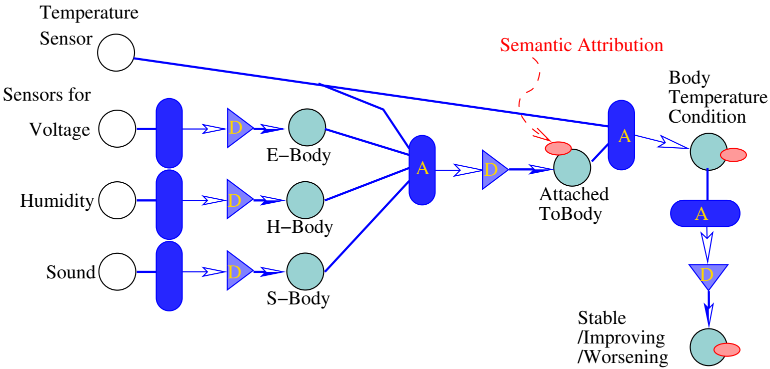


Fantastic
VeryDesirable
Desirable
SomewhatDesirable
Neutral
SomewhatUndesirable
Undesirable
VeryUndesirable
Disaster

+1
0
−1

Semantic Attribution maps the values of a property to a point in the desirability scale.

BioPatch with Semantic Attribution



History

History of a Property The evolution of the values of a property.

Abstracted History The history stores abstracted values.

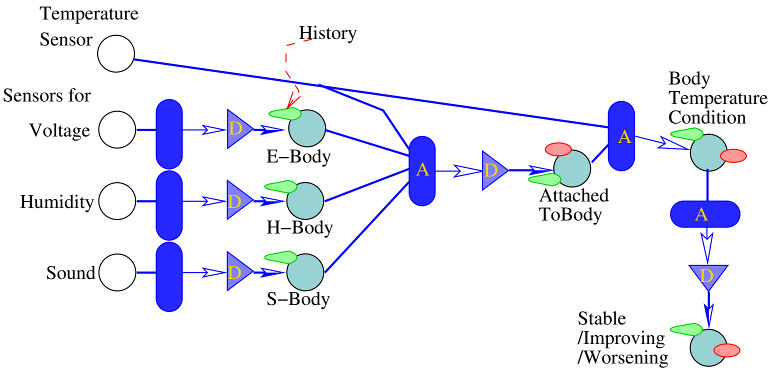
Attributed History The history is annotated with attributions.

Fading History If the property values are more abstracted the longer ago they have occurred.

Consolidating History Relevant memories are enforced, irrelevant memories are cleaned.

Evolving History Memories are adjusted to fit later observations.

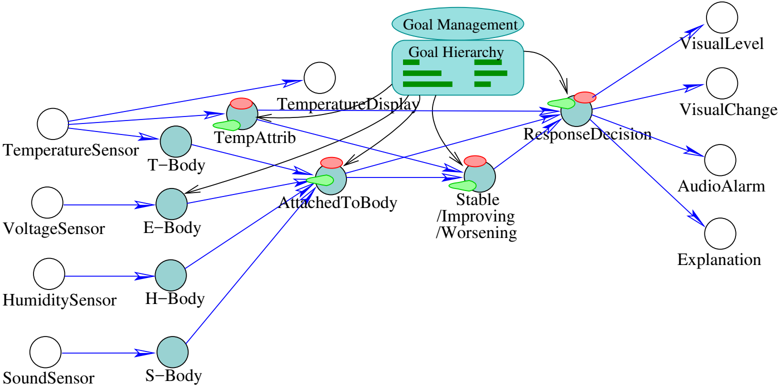
BioPatch with History



Expectations and Goals

- Expectations on Environment
- Expectations on Subject
- Sub-Goals
- Goals
- Purpose

Acting BioPatch

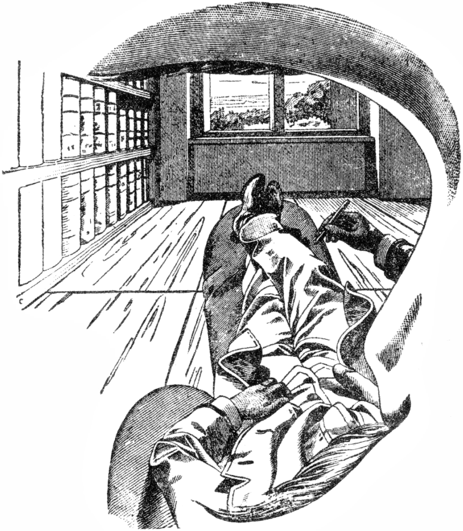


Introspection and Simulation

Self Inspection Engine

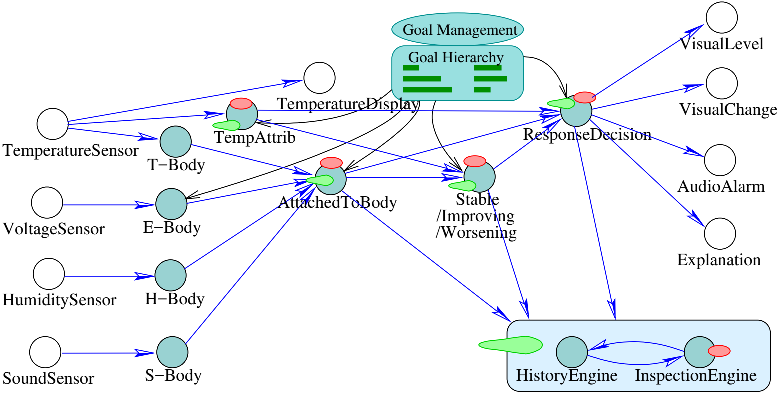
Model Transformation

Simulation

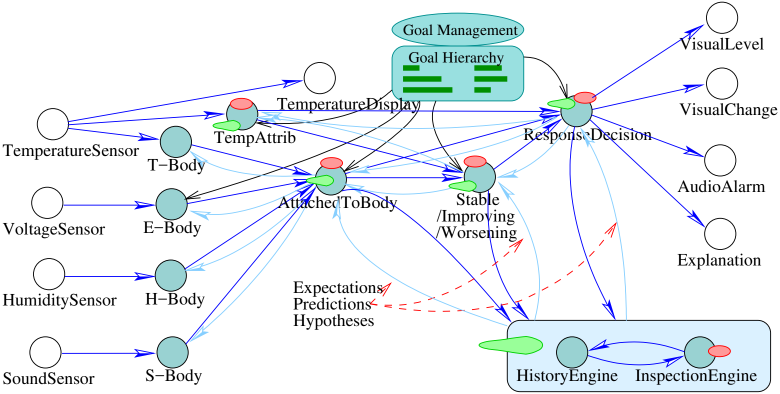


Ernst Mach “Innenperspektive”, 1886

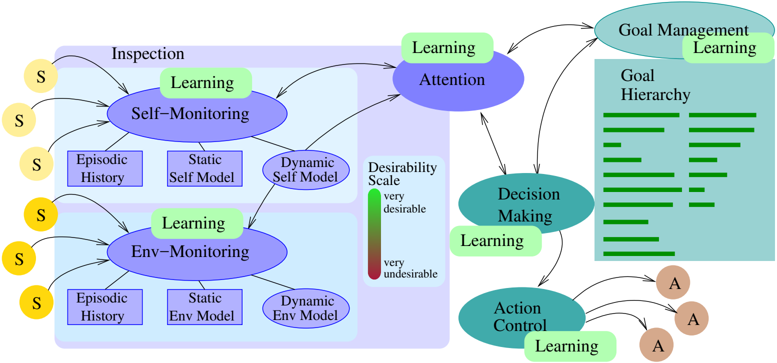
Self-inspecting BioPatch



BioPatch with Top-down Prediction



Self-Awareness Architecture



Cyber-Physical SoC

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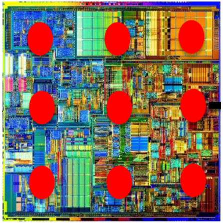
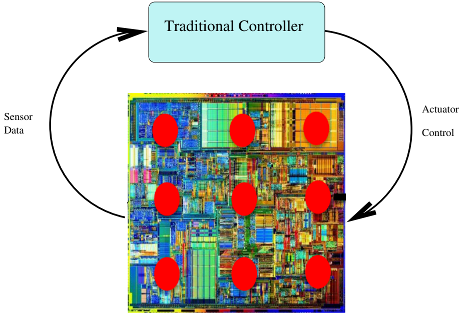


Self-monitoring chip

Cyber-Physical SoC



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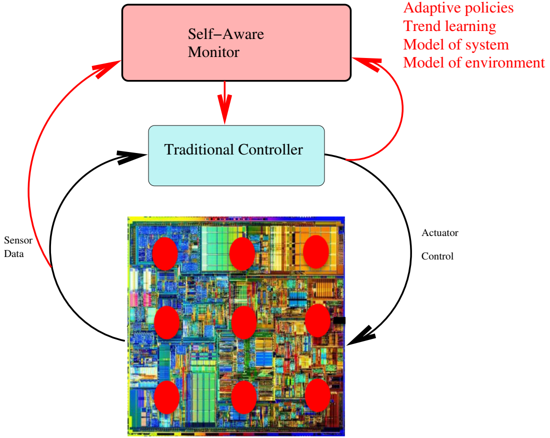
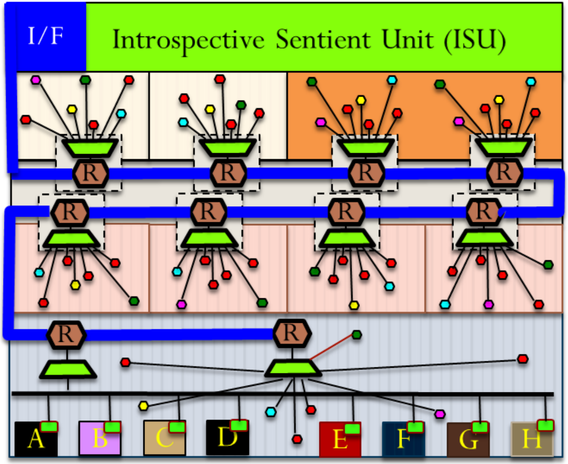


Self-monitoring chip

CPSoC - A Sensor Rich SoC Platform



Santanu Sarma, Nikil Dutt, P. Gupta, A. Nicolau, and N. Venkatasubramanian. “CyberPhysical-System-On-Chip (CPSoC): A Self-Aware MPSoC Paradigm with Cross-Layer Virtual Sensing and Actuation”. In: *Proceedngs of the Design, Automation and Test in Europe Conference and Exhibition (DATE)*. Grenoble, France, Mar. 2015

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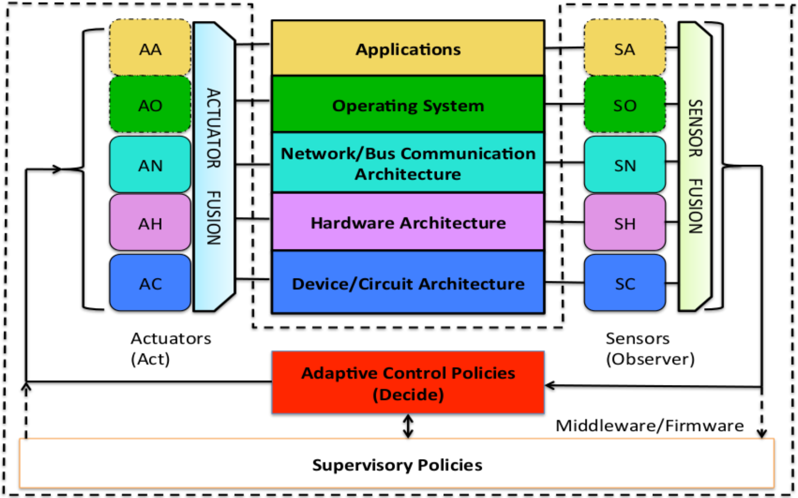
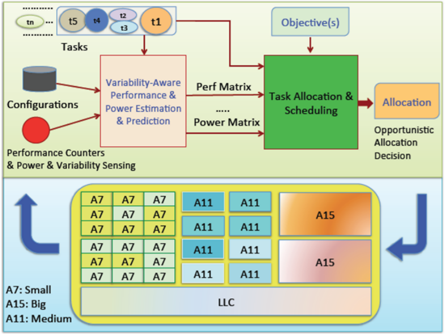
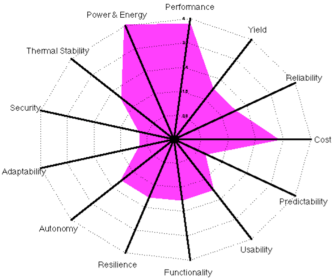


Nikil Dutt, Axel Jantsch, and Santanu Sarma. “Self-Aware Cyber-Physical Systems-on-Chip”. In: *Proceedings of the International Conference for Computer Aided Design*. invited. Austin, Texas, USA, Nov. 2015

Improvement of Energy Efficiency



tn
t5
t4
t2
t3
t1
Tasks
Objective(s)
Configurations
Variability-Aware Performance & Power Estimation & Prediction
Perf Matrix
.....
Power Matrix
Task Allocation & Scheduling
Allocation
Opportunistic Allocation Decision
Performance Counters & Power & Variability Sensing
A7
A11
A15
LLC
A7: Small
A15: Big
A11: Medium

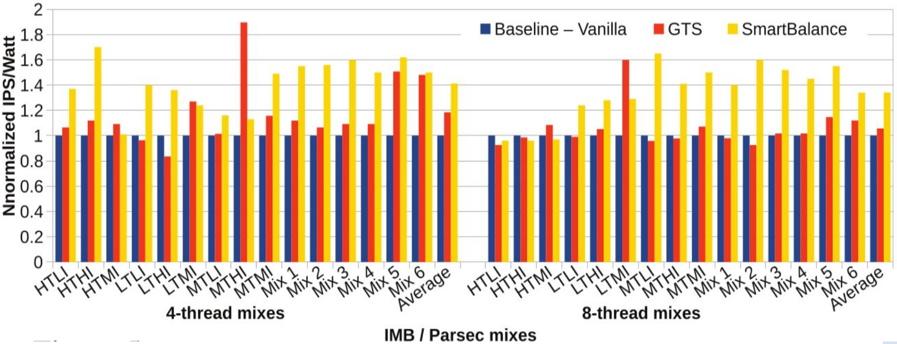


Goal:

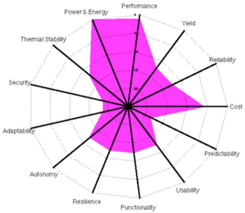
- **Energy Efficiency**

Santanu Sarma and Nikil Dutt. “Cross-Layer Exploration of Heterogeneous Multicore Processor Configurations”. In: *VLSI Design Conference*. 2015

Improvement of Energy Efficiency

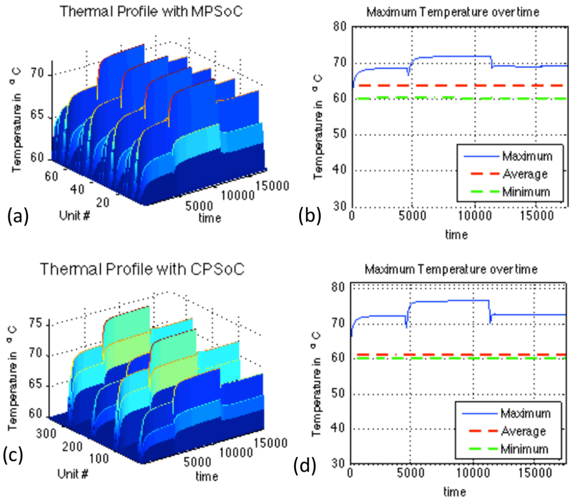


The benefit comes from actually measuring energy efficiency.



Santanu Sarma, T. Muck, L. A.D. Bathen, N. Dutt, and A. Nicolau. "SmartBalance: A Sensing-Driven Linux Load Balancer for Energy Efficiency of Heterogeneous MPSoCs". In: *Proceedings of the Design Automation Conference*. July 2015

Thermal-Aware Performance



Throughput improvement by 70%-300% for same power and temperature.

Benefit is due to accurate and fine-grain measurement and tight tracking.

Santanu Sarma, Nikil Dutt, N. Venkatasubramaniana, A. Nicolau, and P. Gupta. *CyberPhysical-System-On-Chip (CPSoC): Sensor-Actuator Rich Self-Aware Computational Platform*. Tech. rep. CECS Technical Report No: CECS TR–13–06. Irvine, CA 92697-2620, USA: Center for Embedded Computer Systems University of California, Irvine, May 2013.

Hardware Faults

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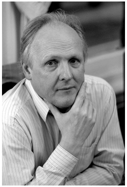
HW Faults



Steve Furber in a keynote at ETS in 2006 predicted that

> within a decade we will see 100 billion transistor chips. That is the good news. The bad news is that 20 billion of those transistors will fail in manufacture and a further 10 billion will fail in the first year of operation.

Steve Furber. “Living with failure: Lessons from nature?” In: *Proceedings of the European Test Symposium (ETS)*. 2006

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What can fail?

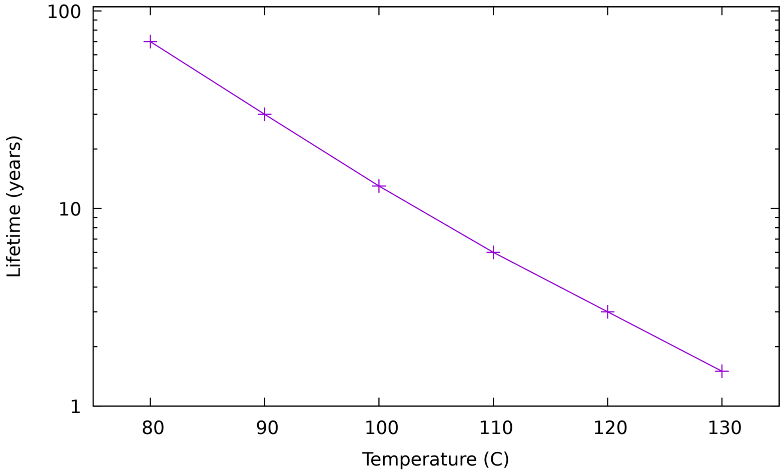
- Sensors
- Computing components
- Communication links
- Actuators
- SoC components

Fault causes and effects

Physical cause		Accelerated by process variation	Fault class	Burstiness
Radiation	Neutrons	No	Transient logic	Yes
	α-particles	No	Transient logic	Yes
Electromagnetic interference	cross coupling of parallel wires	No	Intermittent delay	No
	self coupling, Skin effect leading to higher resistance	No	Intermittent delay	No
Aging	Electromigration	Yes	intermittent → permanent delay and logic fault	No
	Bias Temperature Instability (BTI)	Yes	intermittent → permanent delay fault	No
	Hot carrier injection	Yes	intermittent → permanent delay faults	No
	Oxide breakdown/Time Dependent Dielectric Breakdown (TDDB)	Yes	intermittent → permanent logic fault	No
Power density variation and heat flux	leakage power variation due to temperature differences	Yes	Intermittent → permanent delay and logic faults	Yes
	performance variation due to temperature differences;	Yes	intermittent delay failures	Yes
	variations in wear-out effects due to temperature differences	Yes	intermittent and permanent, delays, opens and shorts	Maybe

Martin Radetzki, Chaochao Feng, Xueqian Zhao, and Axel Jantsch. “Methods for Fault Tolerance in Networks-on-Chip”. In: *ACM Computing Surveys* 46.1 (July 2013), 8:1–8:38

Aging is temperature dependent



Lifetime of an inverter chain decreases by a factor of 2.2 for every 10°C increase in operating temperature due to NBTI.

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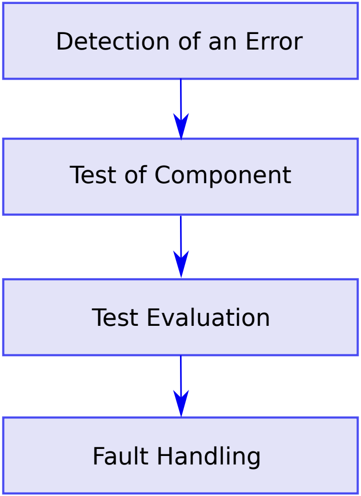
Flow of Diagnosis



Detection of an Error

Error detection codes
Periodic self-test
Modular redundancy

Test of Component

BIST
Initiated by system

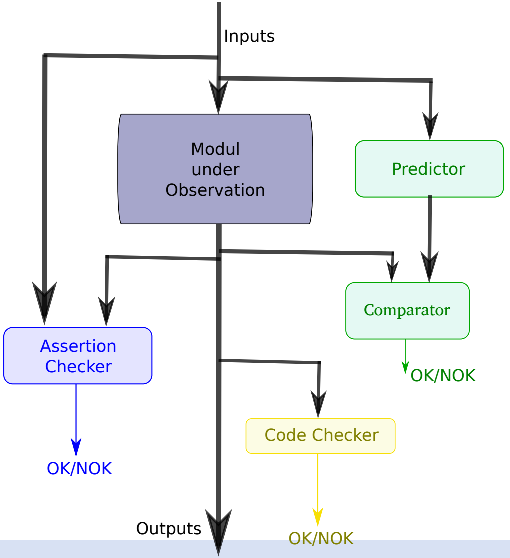
Test Evaluation

Analysis of response
Localization of fault

Fault Handling

Reconfiguration
Update of health map

Monitoring during Operation



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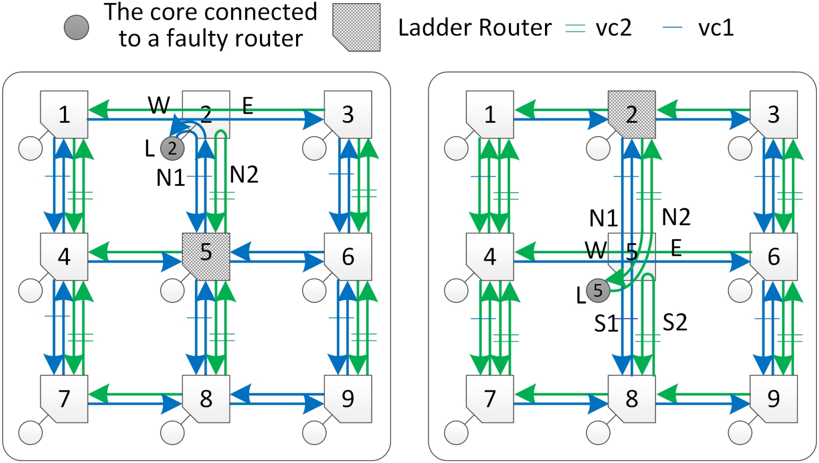
Minimal Intrusion Testing

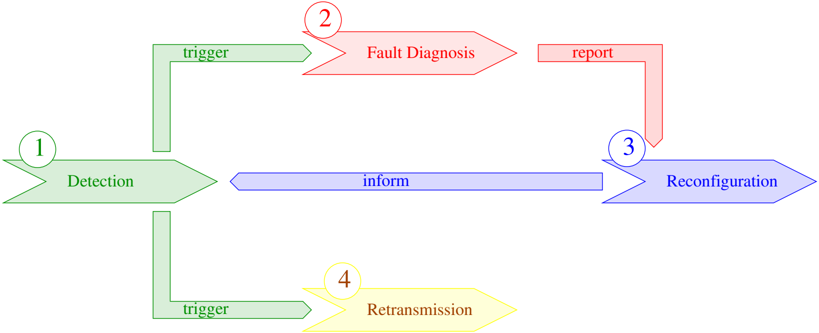


(a)

(b)

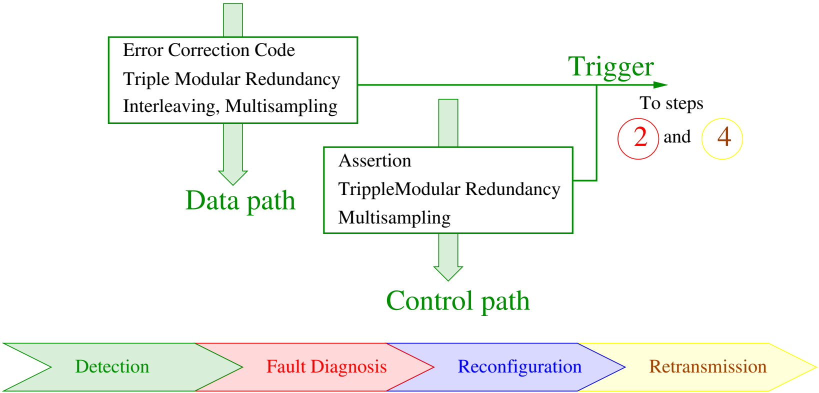
Junshi Wang, Masoumeh Ebrahimi, Letian Huang, Qiang Li, Guangjun Li, and Axel Jantsch. "Minimizing the System Impact of Router Faults by Means of Reconfiguration and Adaptive Routing". In: *Microprocessors and Microsystems* 51 (June 2017), pp. 252–263

NoC Fault Reliability Flow



Junshi Wang, Masoumeh Ebrahimi, Letian Huang, Axel Jantsch, and Guangjun Li. “Design of Fault-Tolerant and Reliable Networks-on-Chip”. In: *IEEE Annual Symposium on VLSI (ISVLSI)*. Montpelllier, France, July 2015

Fault Detection



Error Correction Code

Triple Modular Redundancy

Interleaving, Multisampling

Data path

Assertion

TrippleModular Redundancy

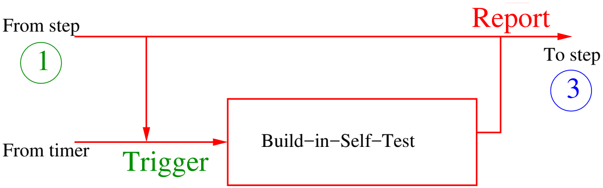
Multisampling

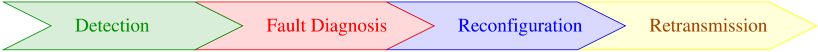
Control path

Trigger

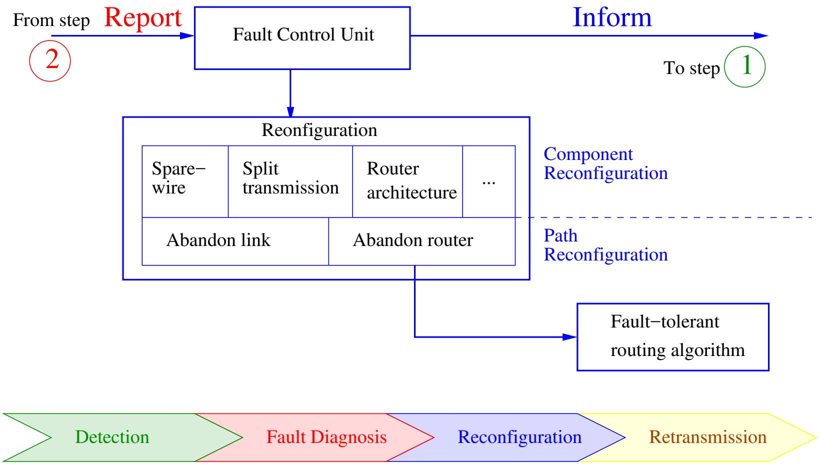
To steps 2 and 4

Fault Diagnosis

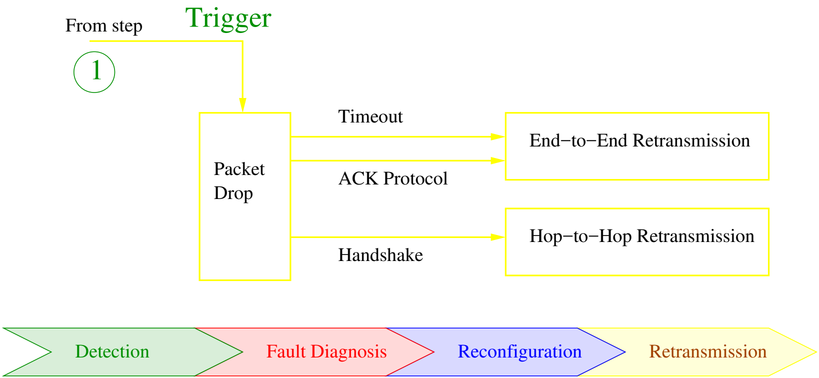




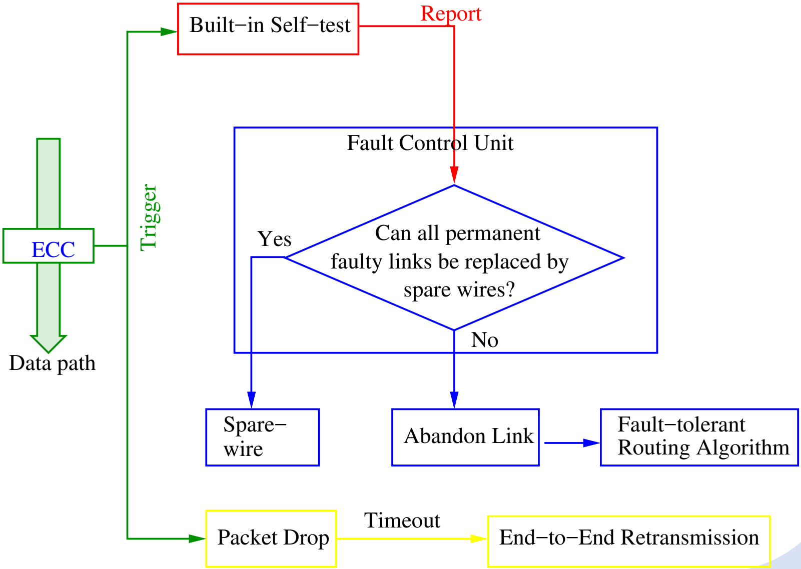
Reconfiguration



Retransmission



Example: Reliability Design for Faulty Links


Built−in Self−test
Report
Fault Control Unit
Can all permanent faulty links be replaced by spare wires?
Yes
No
ECC
Trigger
Data path
Spare−wire
Abandon Link
Fault−tolerant Routing Algorithm
Packet Drop
Timeout
End−to−End Retransmission

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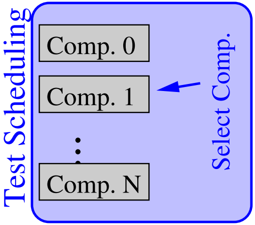
CASP

Concurrent Autonomous Chip Self-Testing using Stored Test Patterns



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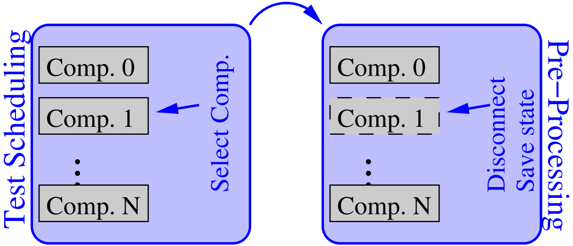

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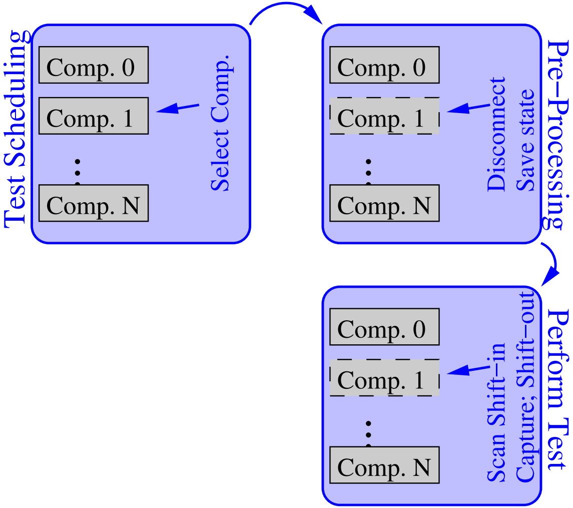

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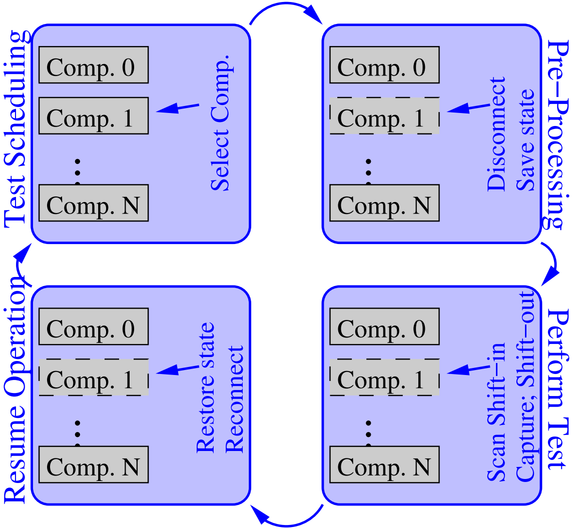

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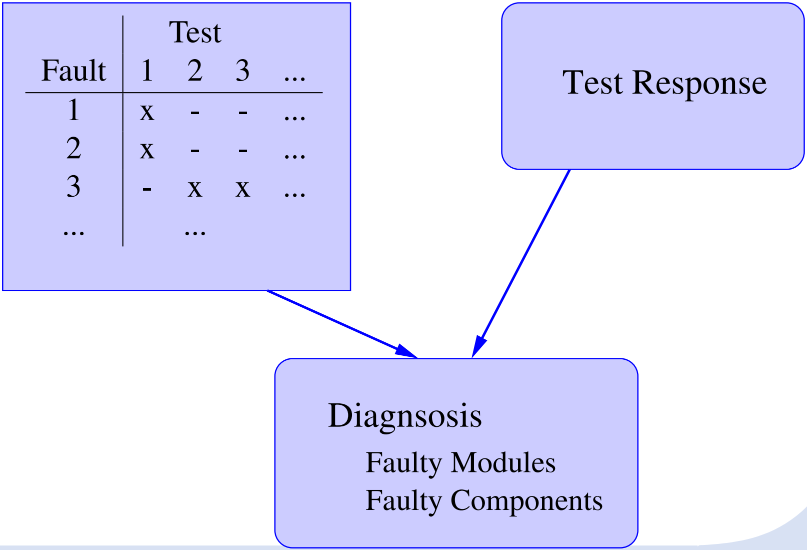
Diagnosis

Fault Dictionary



	Test			
Fault	1	2	3	...
1	x	-	-	...
2	x	-	-	...
3	-	x	x	...
...		...		

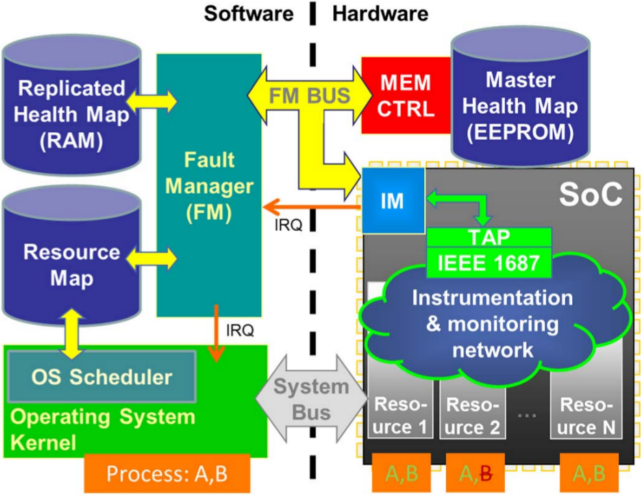
Test Response

Diagnsosis

Faulty Modules

Faulty Components

Health Management



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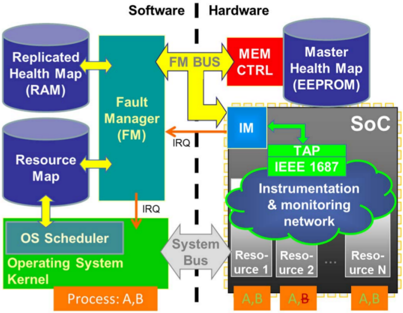
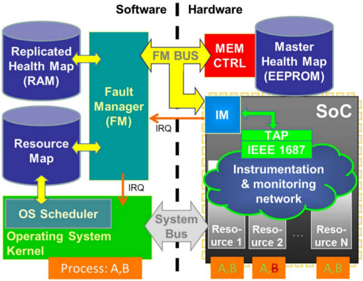
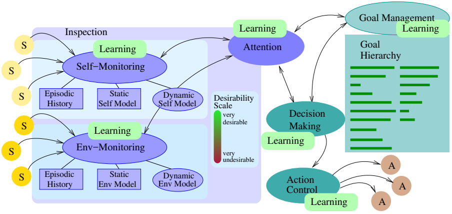
Health Management



- Health Map: detailed information about faults
- Resource Map: List of healthy resources
- Fault Manager: Updates HM and RM
- Instrument Manager: interface to the instrumentation and monitoring network
- Fault detection and diagnosis: Embedded monitors and instrumentation

Self-Awareness for Health Management





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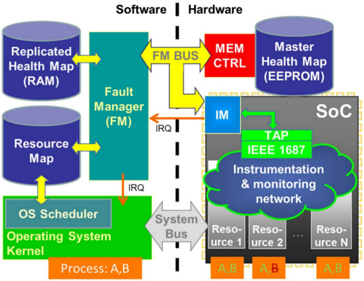

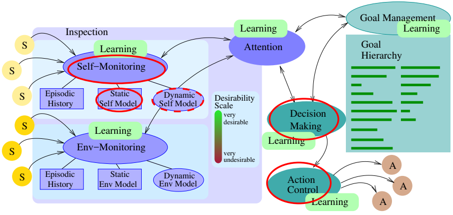

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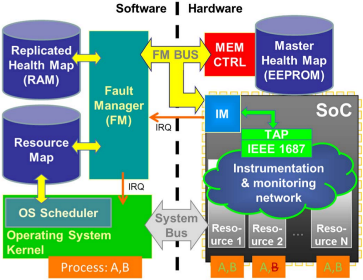

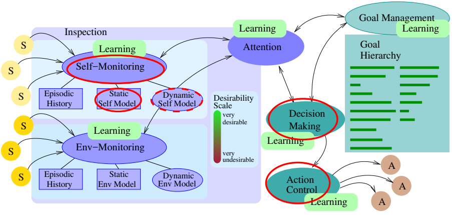

What is missing for Self-Awareness?

- History
- Learning
- Attention
- Goal management
- Comprehensive assessment

Self-Aware Monitoring

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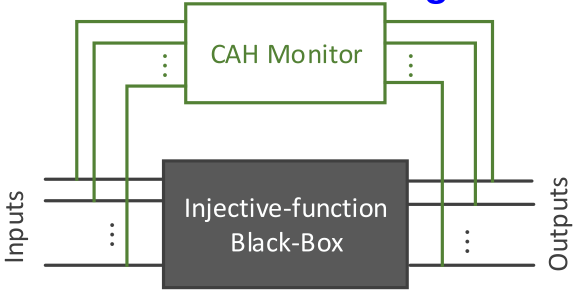
Context Aware Health Monitoring of an AC Motor

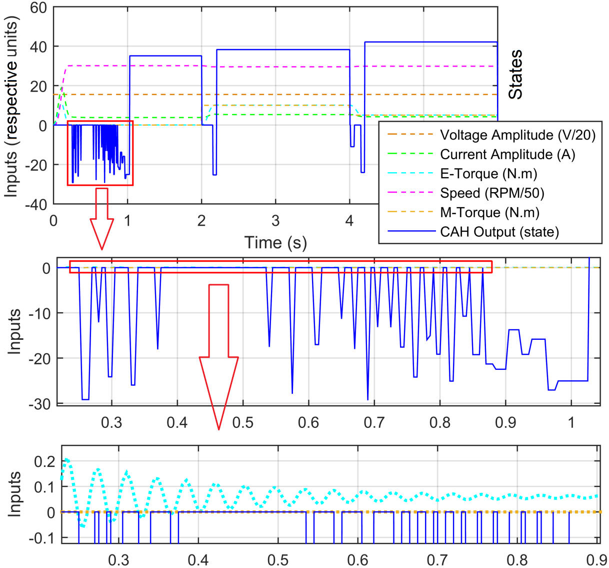


CAH Features

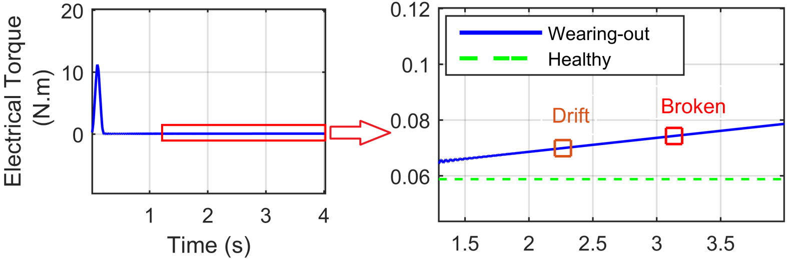
- No Model and minimal assumptions about the system
- Main assumption: injective function
- States are automatically inferred and learned
- Anomalies are detected when injectivity is violated

M. Götzinger, N. TaheriNejad, H. A. Kholerdi, and A. Jantsch. "On the design of context-aware health monitoring without a priori knowledge; an AC-Motor case-study". In: *2017 IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE)*. Apr. 2017, pp. 1–5

CAH Normal Mode



CAH Anomaly Detection



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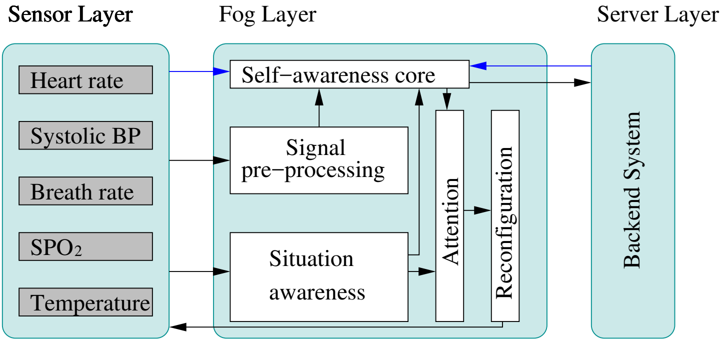
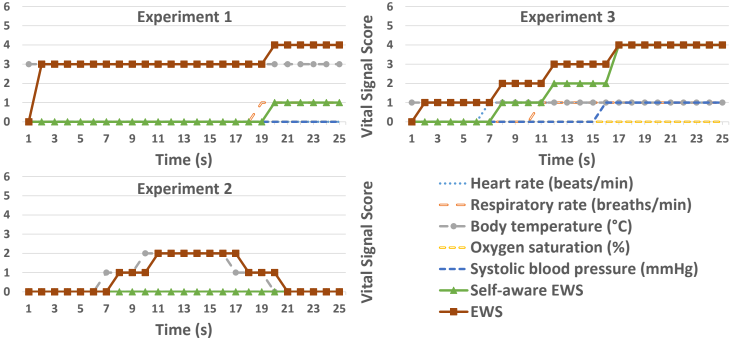
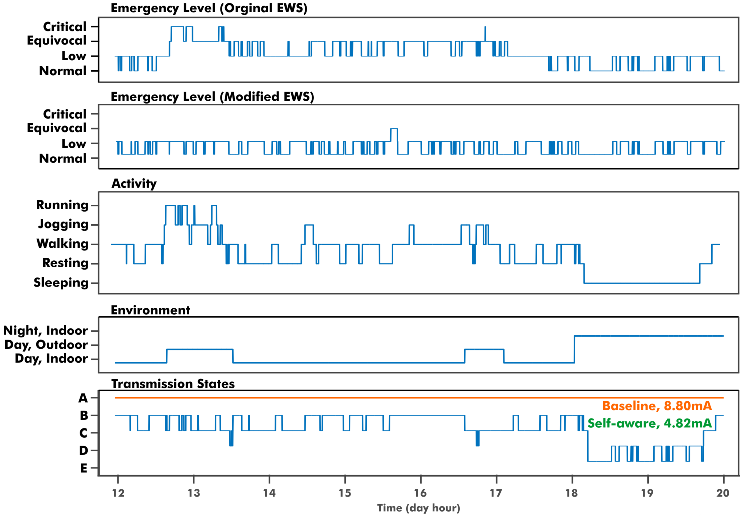
Early Warning Score



Assessing Data Reliability



Situation Awareness



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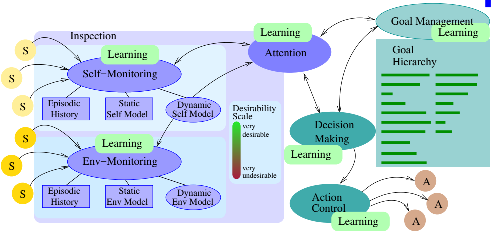
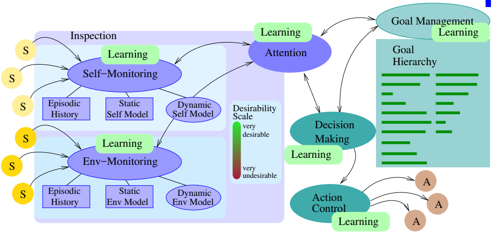
How can Self-Awareness Help?



How can Self-Awareness Help?



- Comprehensive self- and environment monitoring;

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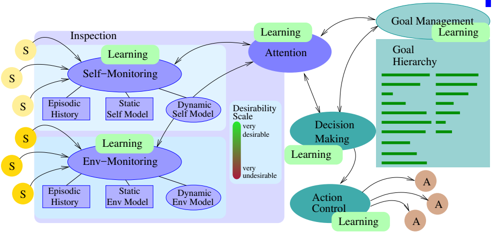

- Comprehensive self- and environment monitoring;
- Formalisms to express all desired and forbidden behavior;

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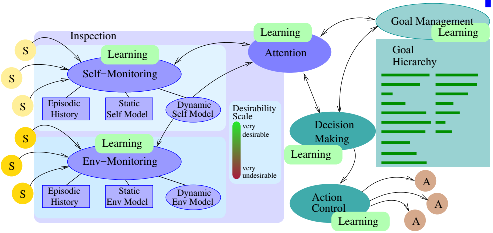

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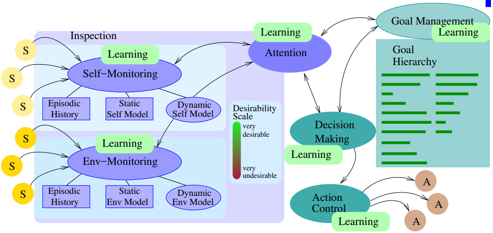

- Comprehensive self- and environment monitoring;
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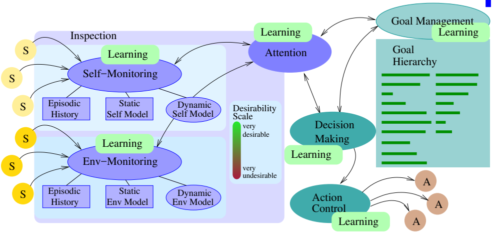

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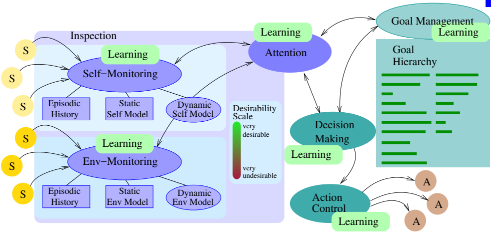

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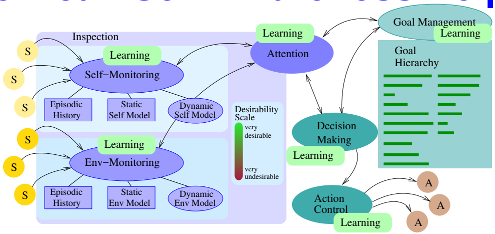

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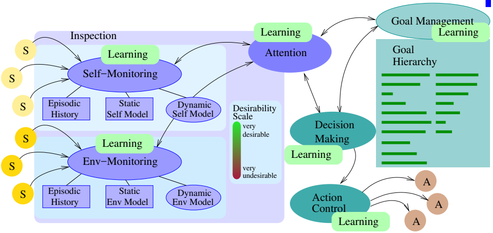

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- Levels of monitoring details (attention directed monitoring);
- Relating anomalies in different domains (desirability scale);
- Comprehensive self- and environment assessment over time;
- Dynamic goal management;
- Learning for continuous adaptation to specific environments, applications, and threats.

Challenges with Self-aware, Adaptive Systems

- How to assess and ensure the quality of sensor data?

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- How to quantify uncertainty, dynamicity, and variability in the platform, the environment, and the applications?

Challenges with Self-aware, Autonomous, Adaptive SoCs

- How to reconcile autonomy with safety critical and real-time systems?

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- How to handle a dynamic hierarchy of goals?

Challenges with Self-aware, Autonomous, Adaptive SoCs

- How to make goal management lightweight?

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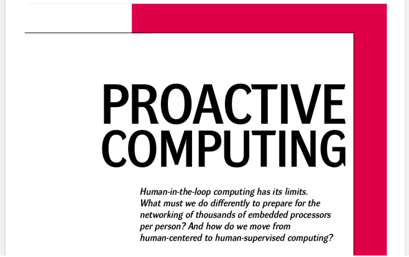
- .....

Let’s Get Out



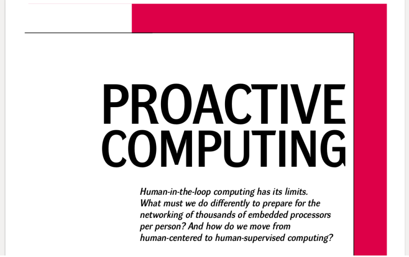
PROACTIVE COMPUTING

Human-in-the-loop computing has its limits. What must we do differently to prepare for the networking of thousands of embedded processors per person? And how do we move from human-centered to human-supervised computing?

David Tennenhouse. “Proactive Computing”. In: *Communications of the ACM* 43.5 (May 2000), pp. 43–50

Let’s Get Out

- Let’s get physical



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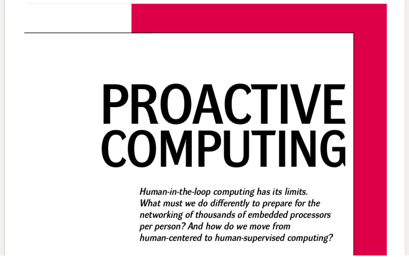
Let’s Get Out

- Let’s get physical
- Let’s get real



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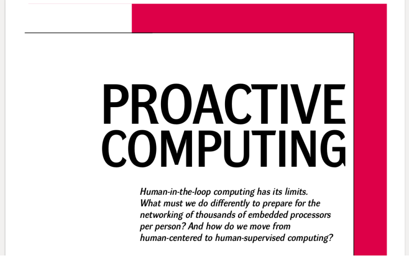
Let’s Get Out

- Let’s get physical
- Let’s get real
- Let’s get out



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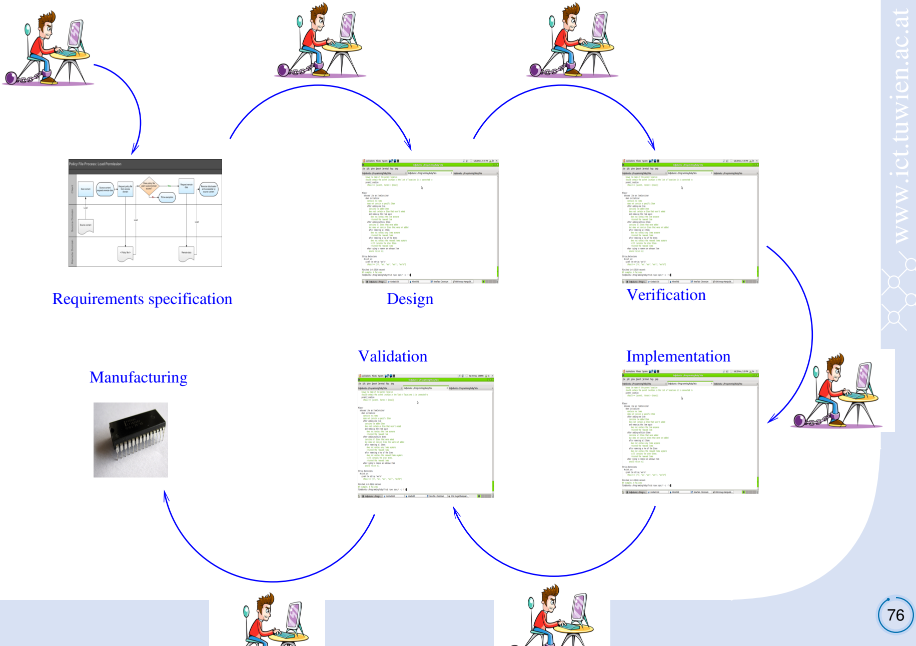
Traditional Design Flow



Requirements specification

Design

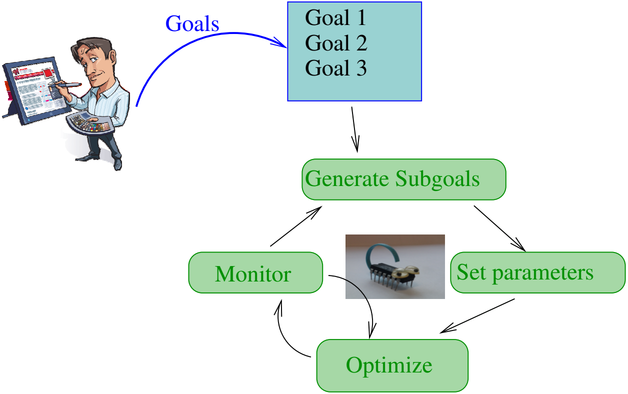
Verification

Implementation

Validation

Manufacturing

Design of Self-Aware Chips



Goals

Goal 1
Goal 2
Goal 3

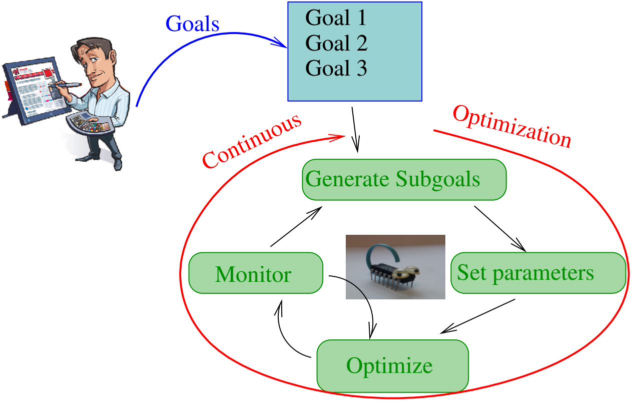
Generate Subgoals

Set parameters

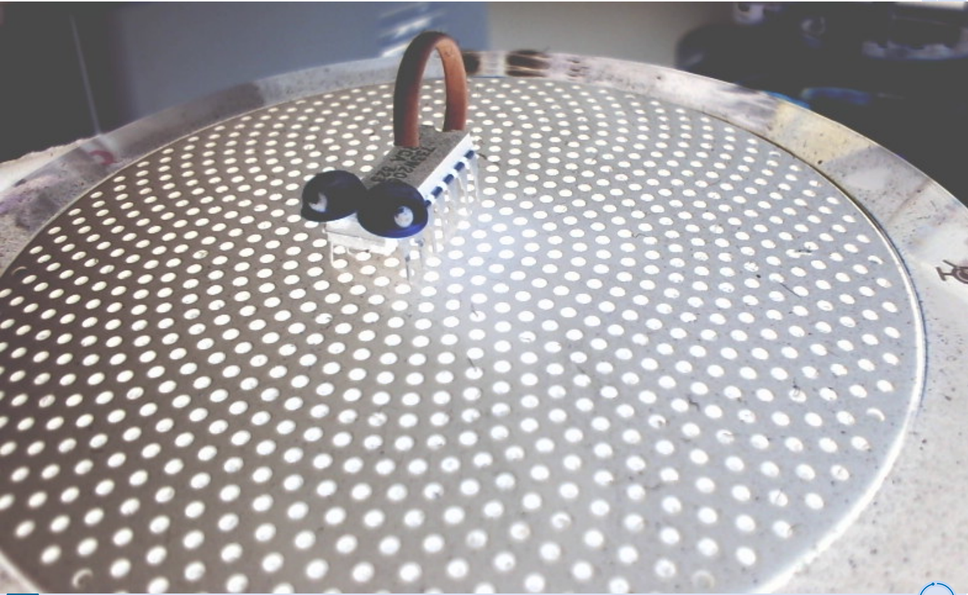
Optimize

Monitor

Design of Self-Aware Chips



Questions ?



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