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Resource Management for Mixed-Criticality Systems on Multi-Core Platforms with Focus on Communication

Embedded Tutorial

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Outline

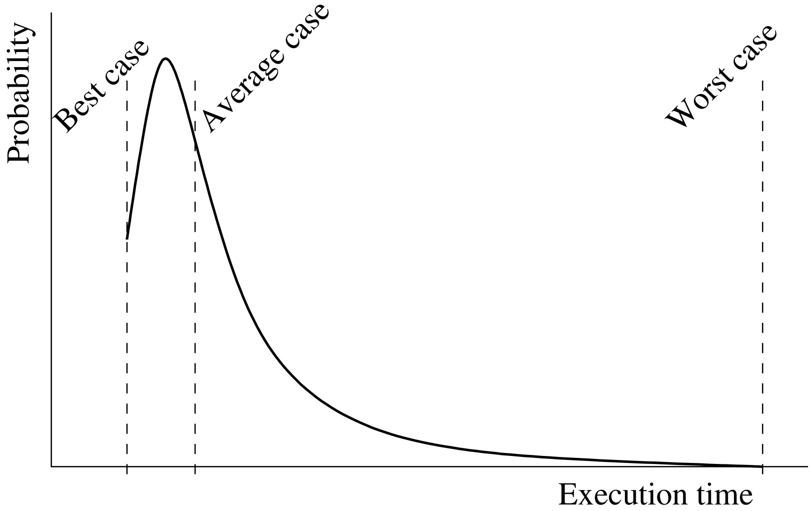
Resource Management for Mixed-Criticality Systems

Mixed Criticality Systems

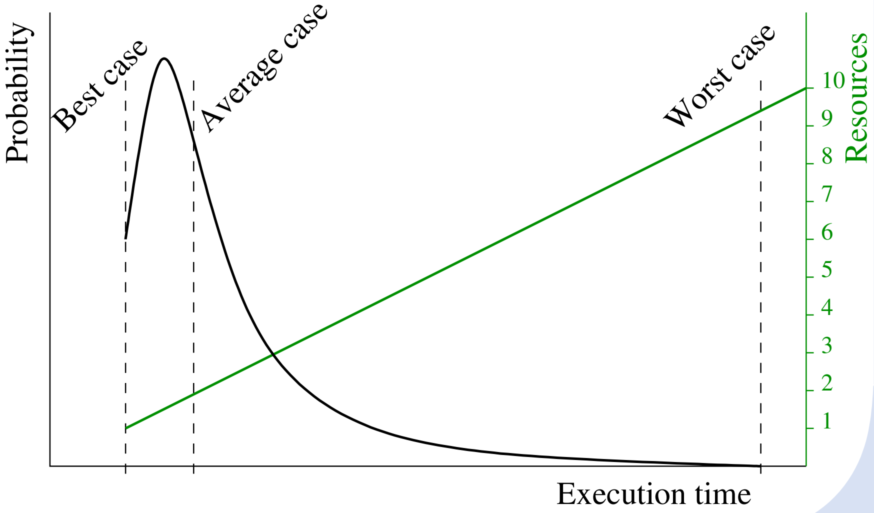
Types of tasks:

Best Effort	May take as long as needed;
Soft Real-Time	Have deadlines, but may miss some deadlines;
Hard Real-time	No deadline must be missed, ever.

Average Case and Worst Case



Average Case and Worst Case



Sharing and Isolation

- **Full Isolation** to accommodate the worst case:
    - Dedicated resources for a given task;
    - Addresses real-time and safety requirements;
    - Costly due to over-provisioning;
    - Complete isolation = no interference.

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  - Best average performance for given cost;
  - Lowest cost for target average performance;
  - Highest efficiency;
  - Unbounded worst case performance.

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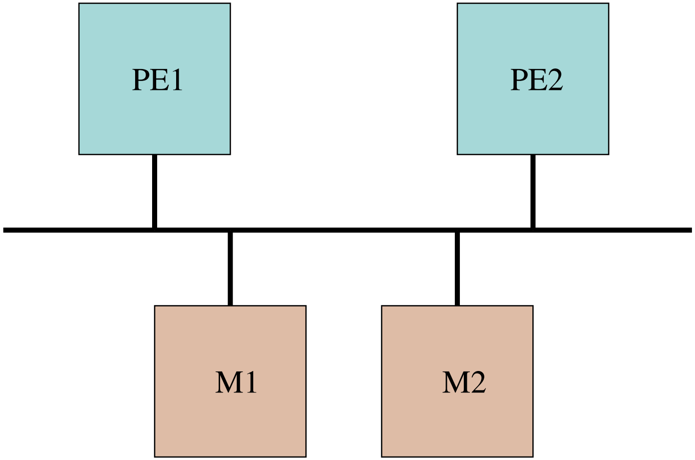
  - Unbounded worst case performance.
- Sharing with **bounded interference**:
  - Allowing and controlling interference can provide real-time and safety requirement;
  - Reduced costs;
  - Applicable for mix of critical and best effort tasks.

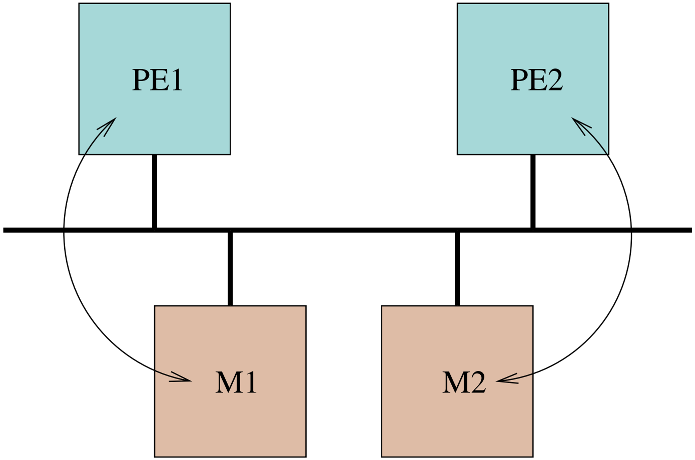
Interference Effects

- Direct interference and competition for the same resource;
- Indirect interference through shared resources:
    - Performance inversion,
    - Over-synchronization.

Performance Inversion

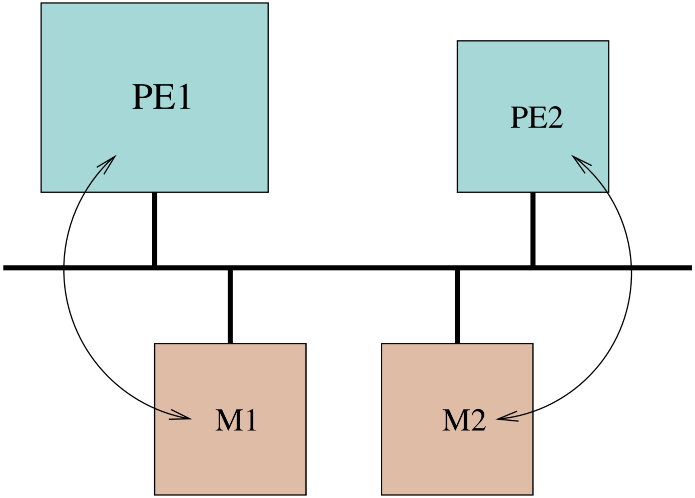


Performance Inversion



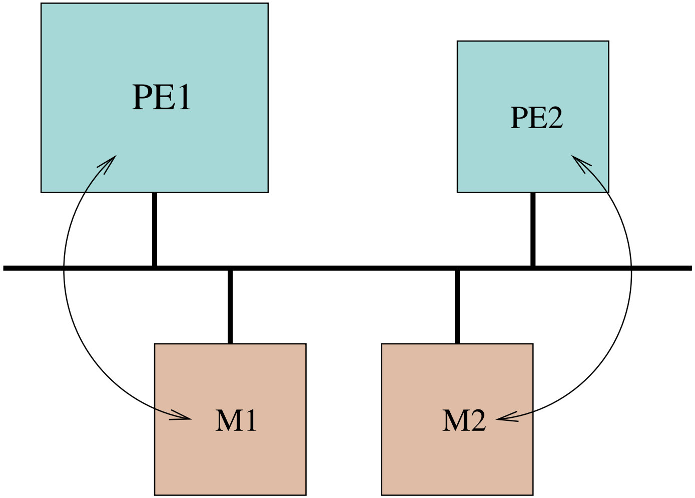
- PE1 communicates with M1 and PE2 communicates with M2;
- All tasks meet deadlines;

Performance Inversion



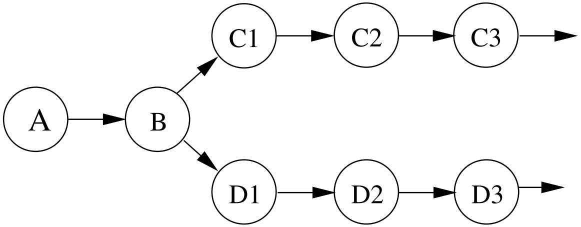
- Replacing PE1 with a faster PE;

Performance Inversion



- Replacing PE1 with a faster PE;
- **May increase execution time of PE2 tasks.**

Over-Synchronization



- Assumption: Bounded buffers between tasks;
- No control or data dependency between C and D branches;

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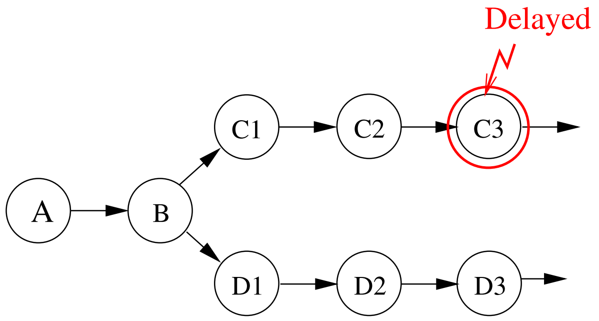

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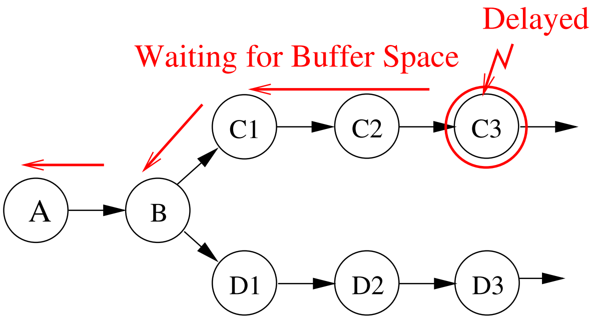

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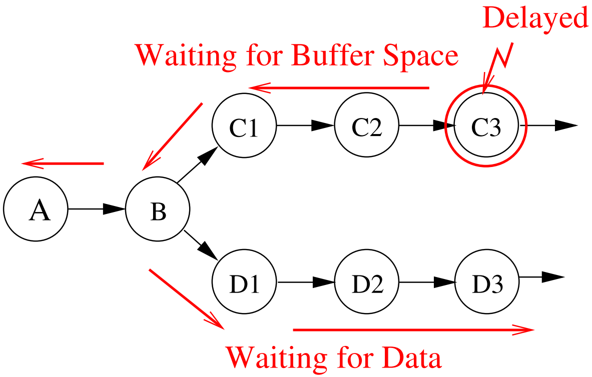
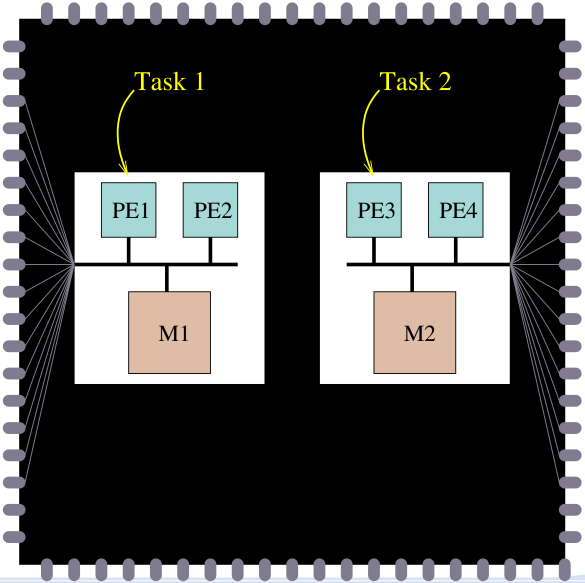


- Assumption: Bounded buffers between tasks;
- No control or data dependency between C and D branches;
- **If C is delayed or stuck, D suffers.**

Spatial and Temporal Isolation

- Spatial isolation: No sharing at any time;
- Temporal isolation: Sharing at pre-defined time periods.

Spatial Isolation



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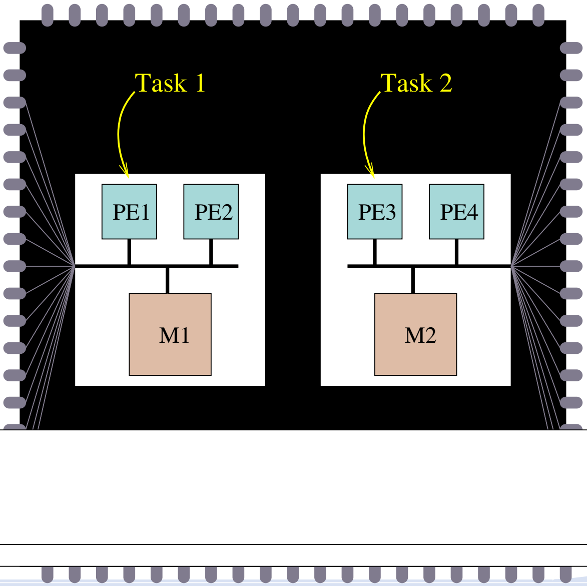
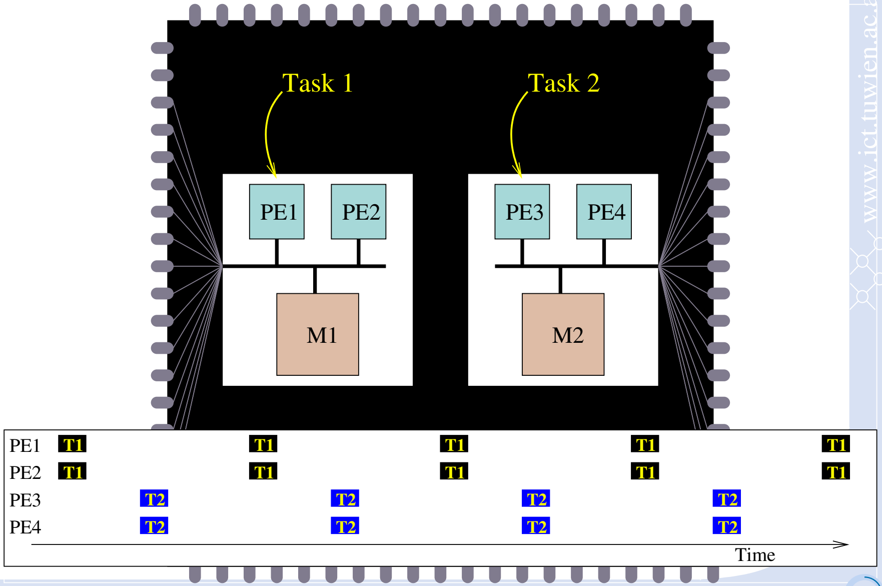
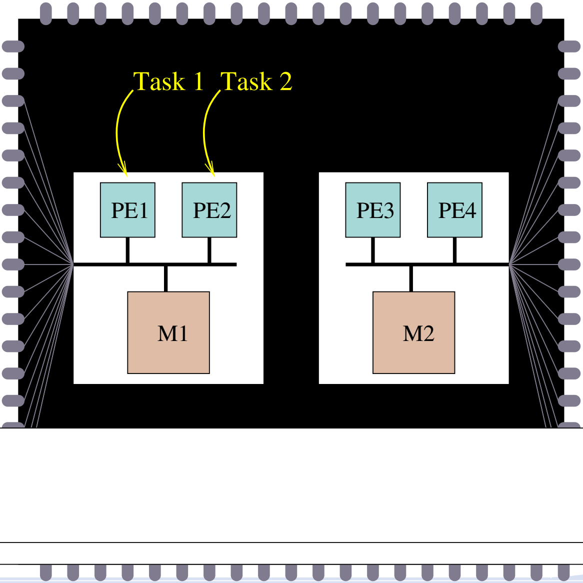


PE1
PE2
PE3
PE4
Time

Spatial Isolation



Temporal Isolation



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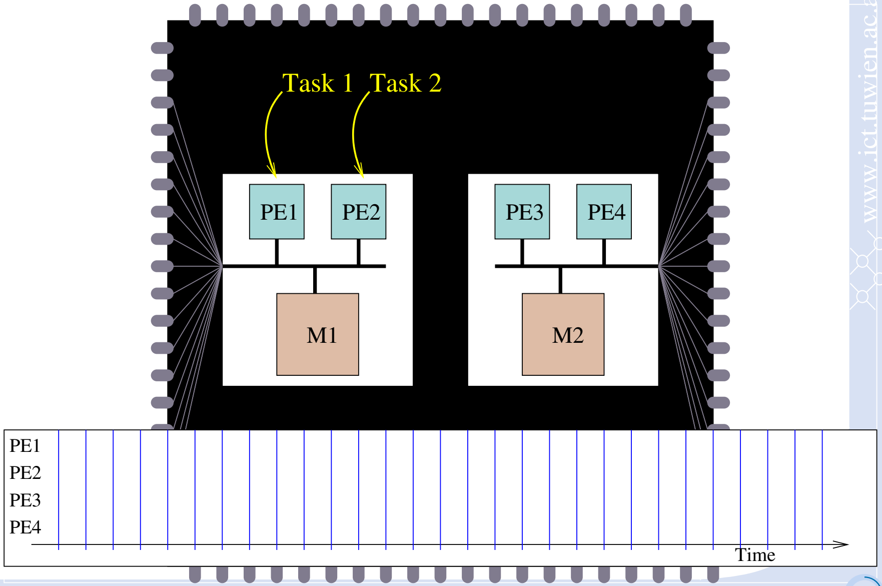

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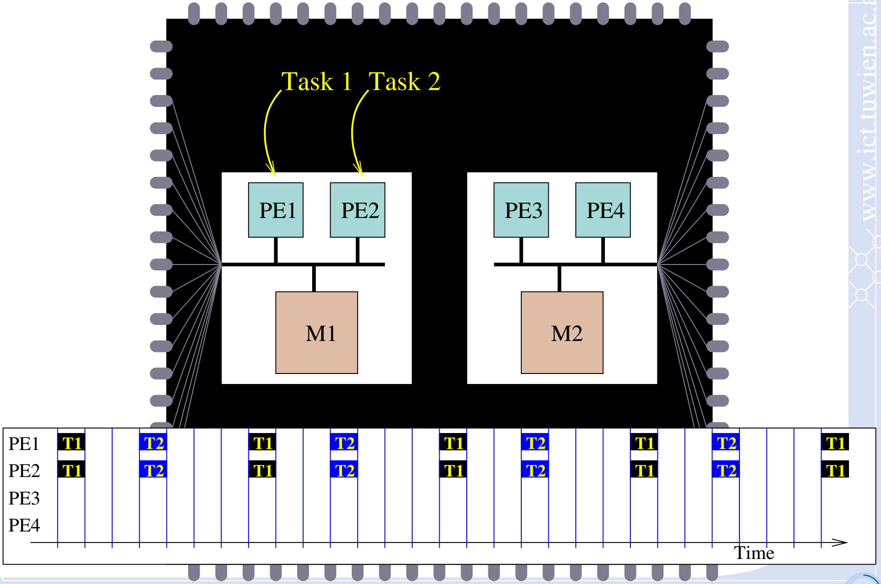

Resource Management in Many-Core SoCs

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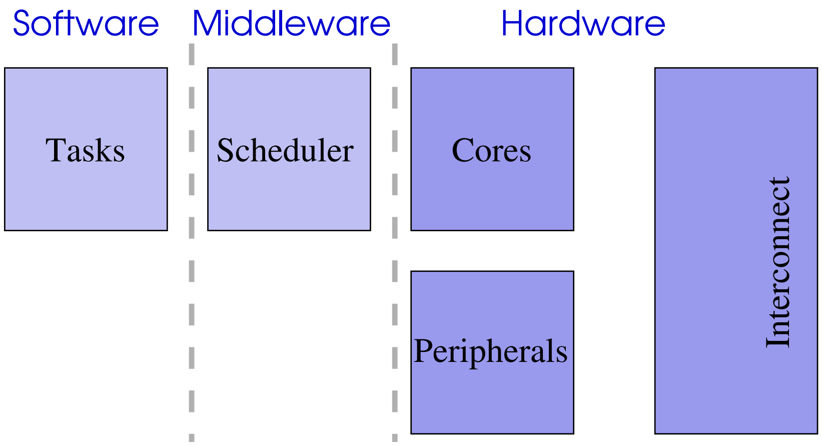
- Many resources lead to a huge design space;
- Types of Resources:
    - Computation: Processing elements,
    - Storage: Buffers, caches, off-chip memory,
    - **Communication: Buses, links, NoCs.**

Overview


Software
Middleware
Hardware
Tasks
Scheduler
Cores
Peripherals
Interconnect

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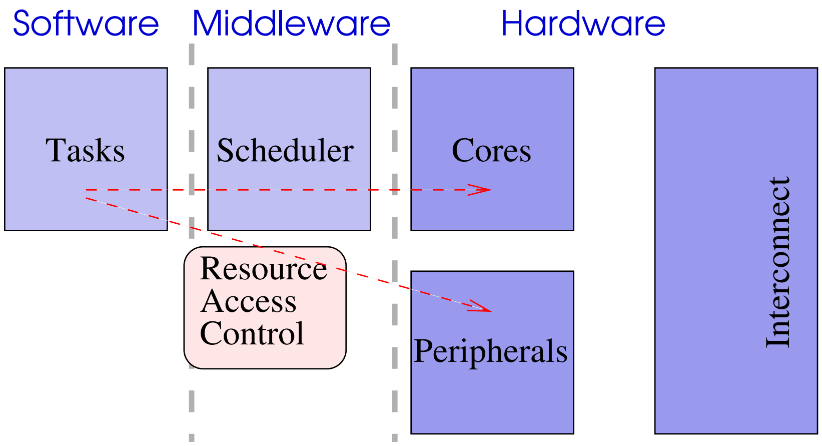
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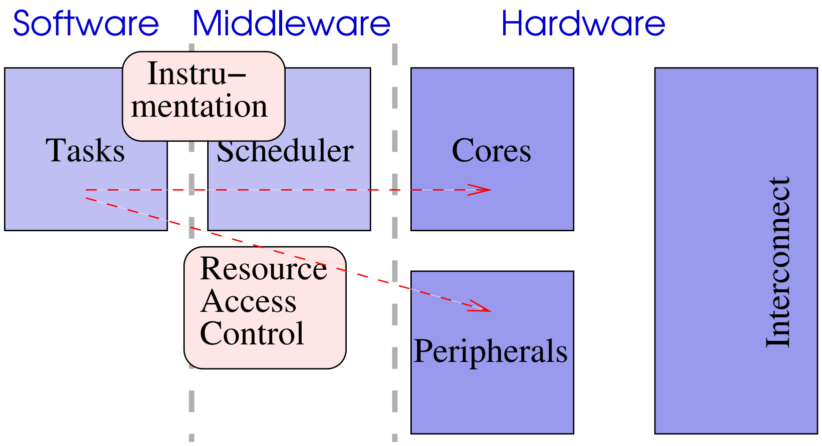
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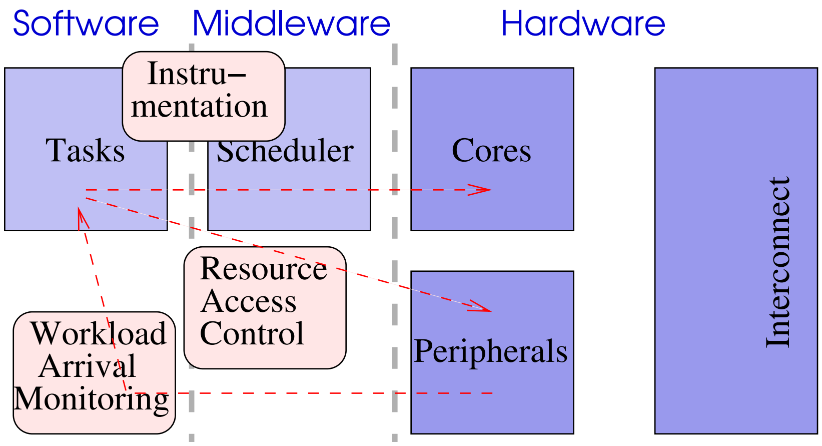
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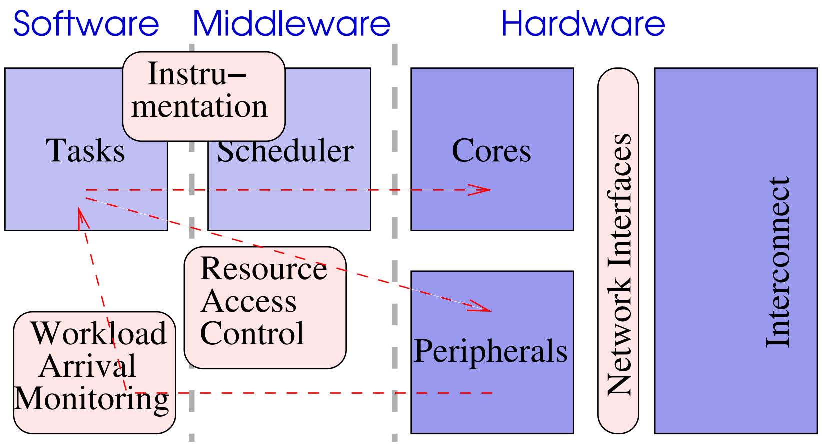
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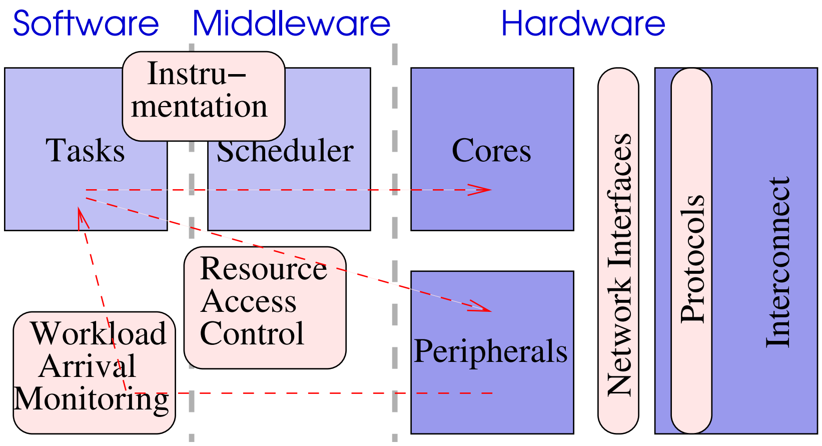
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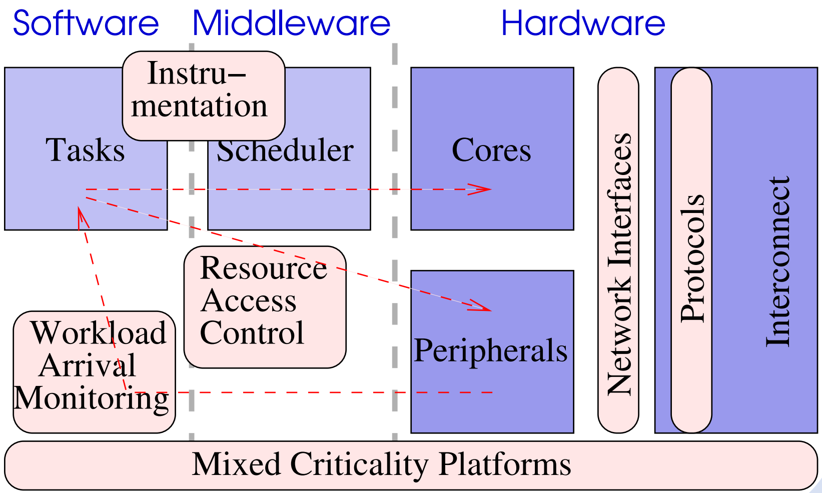

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Monitoring
Mixed Criticality Platforms

Resource Management for Mixed-Criticality Systems

Real-Time Systems

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Real-Time Constraints from Event to System Response

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- Deadlines based on real-time requirements

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Real-Time Constraints from Event to System Response

- Deadlines based on real-time requirements
- No deadline misses allowed ever
- Prepare for the worst-case

Real-Time Systems – Scheduling Example

Task Set

Task	Period	Deadline	WCET
$T1$	10	5	4
$T2$	10	10	6

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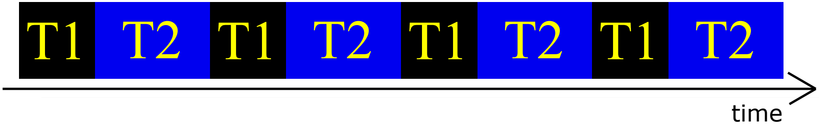

Real-Time Systems – Scheduling Example

Task Set

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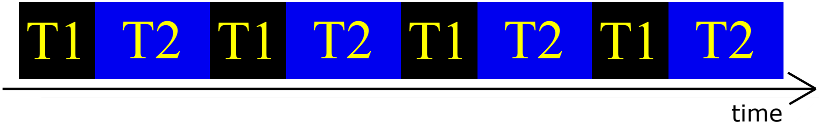

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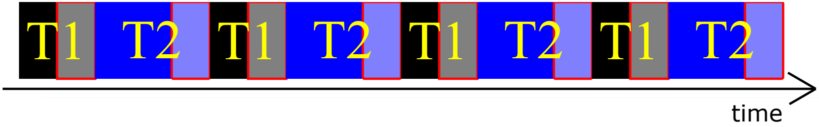
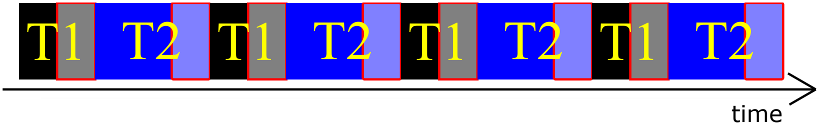
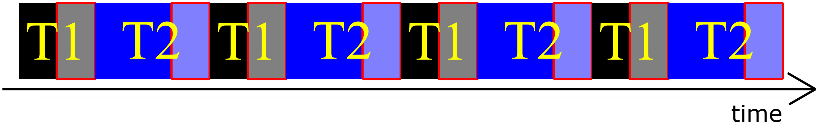


Real-Time Systems – Pros and Cons



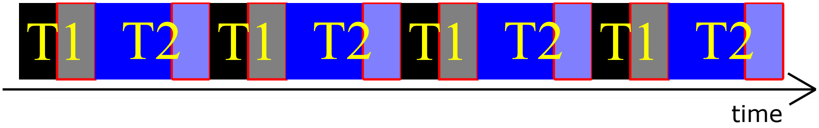
Real-Time Systems – Pros and Cons

- Static guarantees even for the worst-case



Real-Time Systems – Pros and Cons

- Static guarantees even for the worst-case
- Overprovisioning for the average-case



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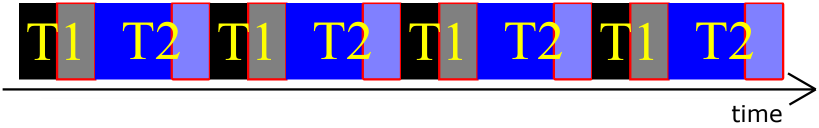

Economic need for trading off guarantees for utilization

Resource Management for Mixed-Criticality Systems

Mixed Criticality Levels

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Worst-Case Execution Time Estimates

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Worst-Case Execution Time Estimates

- Various components are validated against various assumptions

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Worst-Case Execution Time Estimates

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Criticality Levels of Tasks

- Strictness of assumptions

Mixed Criticality Levels

Worst-Case Execution Time Estimates

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Criticality Levels of Tasks

- Strictness of assumptions
- Ordered set of levels

Mixed-Criticality Scheduling with Criticality Mode Switches

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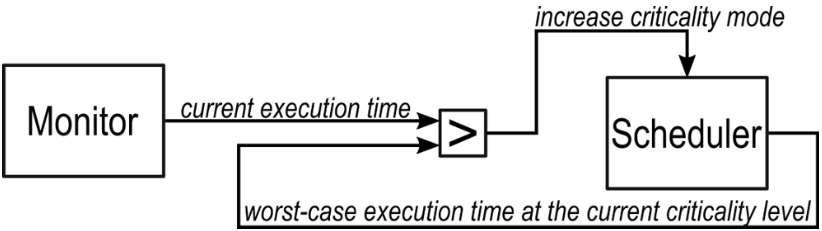
increase criticality mode
Monitor
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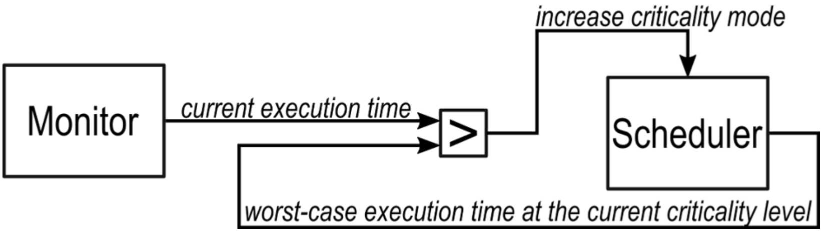
Scheduler
worst-case execution time at the current criticality level

Mixed-Criticality Scheduling with Criticality Mode Switches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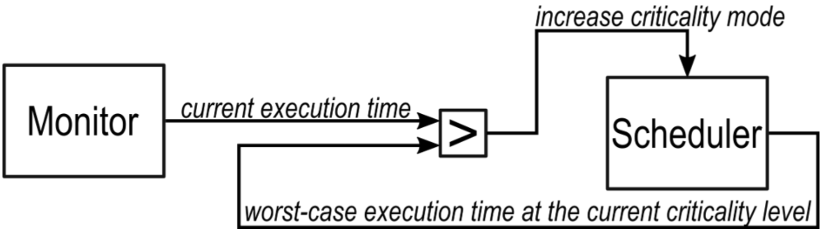
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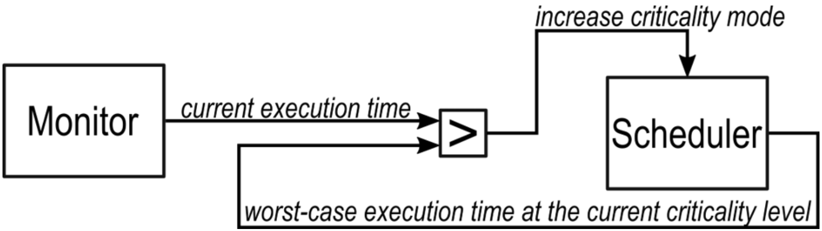
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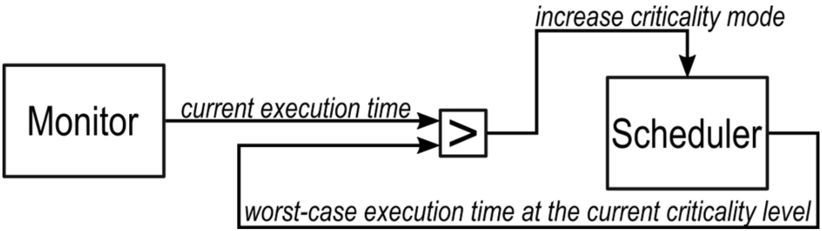
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- Start system in the lowest criticality mode
- Schedule tasks with criticality not below the current criticality mode
- Monitor whether execution violates current assumptions
- Switch to higher criticality mode for stricter assumptions

Mixed-Criticality Scheduling with Mode Switches

Task Set *HI*

Task	Period	Deadline	WCET
$T1$	10	5	4
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Mixed-Criticality Scheduling with Mode Switches

Task Set *HI*

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Task Set *LO*

Task	Period	Deadline	WCET
$T1$	10	5	2
$T2$	10	10	4
$T3$	10	9	3

Mixed-Criticality Scheduling with Mode Switches

Mixed-Criticality Task Set

Task	CL	Period	Deadline	WCET
$T1$	HI	10	5	$[2, 4]$
$T2$	HI	10	10	$[4, 6]$
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Mixed-Criticality Scheduling with Mode Switches

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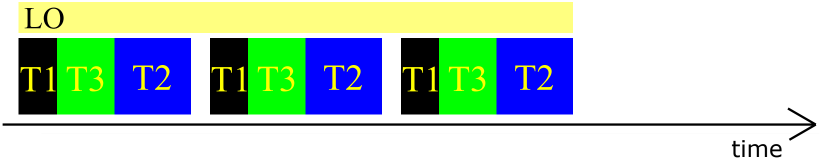

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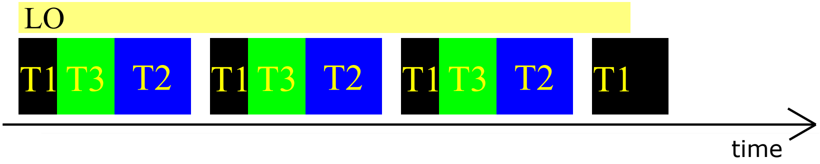

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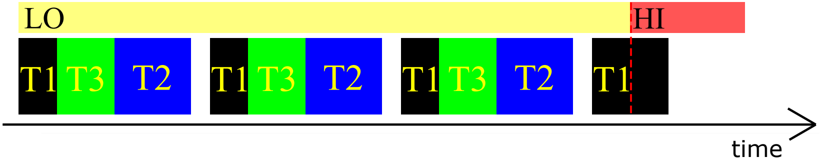

Ignoring *LO* criticality tasks in *HI* mode

Mixed-Criticality Scheduling with Mode Switches

Mixed-Criticality Task Set

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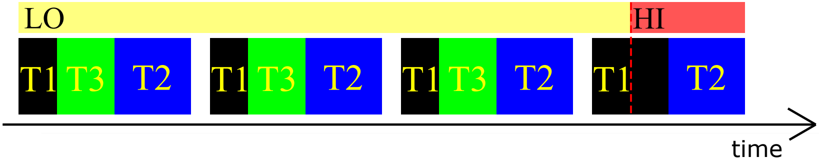

Ignoring *LO* criticality tasks in *HI* mode

Limitations of Mode Switching Scheduling

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Static Verification

Runtime Robustness

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- Timing guarantees for each mode

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Runtime Robustness

- Switching mode to restrict assumptions as necessary

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Static Verification

- Timing guarantees for each mode
- **No link to requirements of safety standards**

Runtime Robustness

- Switching mode to restrict assumptions as necessary
- **Ignoring low-criticality tasks**

Limitations of Mode Switching Scheduling

Static Verification

- Timing guarantees for each mode
- **No link to requirements of safety standards**

Runtime Robustness

- Switching mode to restrict assumptions as necessary
- **Ignoring low-criticality tasks**
- **Returning to low-criticality mode**

Resource Management for Mixed-Criticality Systems

Memory Accesses and Execution Time

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Cache Misses

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- Memory needs to be accessed

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Limited Interference for Critical Tasks

Memory Accesses and Execution Time

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Limited Interference for Critical Tasks

- Reduce WCET of critical tasks by limiting interference

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Limited Interference for Critical Tasks

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- Budget of cache misses for non-critical tasks (cores)

Memory Accesses and Execution Time

Cache Misses

- Memory needs to be accessed
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Limited Interference for Critical Tasks

- Reduce WCET of critical tasks by limiting interference
- Budget of cache misses for non-critical tasks (cores)
- Suspend execution of tasks with depleted budget

Memory Accesses and Execution Time

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- Critical tasks may be penalized by interference

Limited Interference for Critical Tasks

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- Budget of cache misses for non-critical tasks (cores)
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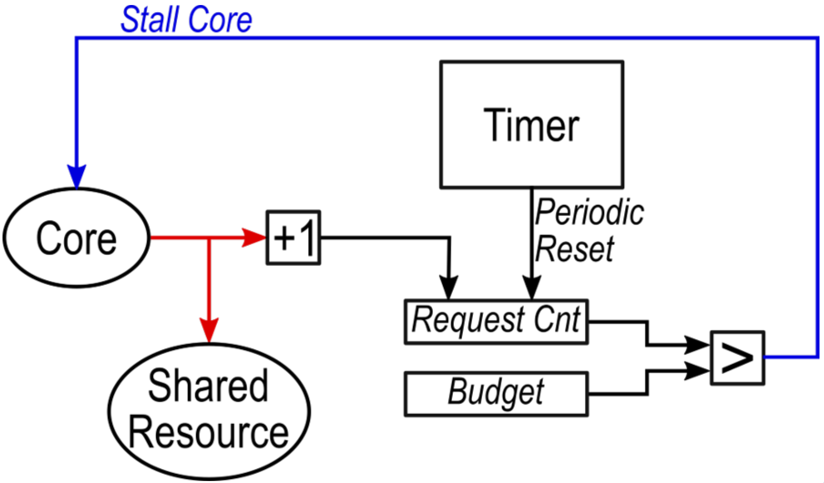
Can be generalized to any shared resource

Memory Access Budgeting



Memory Access Budgeting – Pros and Cons

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Resource Management for Mixed-Criticality Systems

Monitoring Execution Time and Remaining WCET

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WCET and Observation Points for Critical Tasks

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Safety Condition at each Observation Point

The critical task will not miss its deadline even if worst-case happens until the next observation point

Execution Time Monitoring

Evaluate safety condition at each observation point:

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code segment $k-$

code segment k

code segment $k+$

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code segment $k-$		execution time
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code segment k	$+$	$WCET_{interference}(k, k+1)$
observation point $k+1$		
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	$+$	observation overhead
	$<$	deadline

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	$+$	observation overhead
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Suspend non-critical tasks if safety condition does not hold.

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- Large execution time overhead of monitoring

Resource Management for Mixed-Criticality Systems

Workload Arrival Monitoring

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Workload Arrival Function (WAF) for each Task

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Individual WAFs enforce interference bounds between real-time tasks

Group Monitoring Scheme

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- Pareto interface tuples with maximized individual WAFs

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- **Event-triggered**

Workload Arrival Monitoring – Pros and Cons

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- **Considering worst-case is highly pessimistic**

Workload Arrival Monitoring – Pros and Cons

Properties

- **Event-triggered**
- **Considering worst-case is highly pessimistic**
- **Group monitoring provides more accurate assumptions**

Resource Management for Mixed-Criticality Systems

Goals of Mixed-Criticality Communication Protocols

Resource Utilization

- Enable the derivation of tight latency bounds for guaranteed latency traffic
- Analyzable in terms of schedulability

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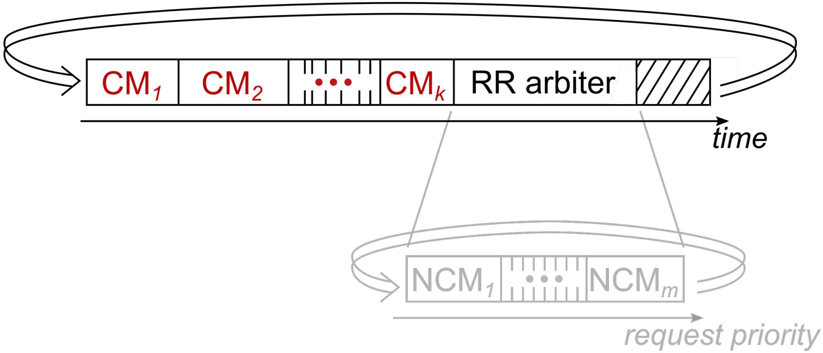
Scalability

- Scale well with the number of bus masters or NoC nodes

TDMA-RR Dual Layer Arbiter

- First layer : TDMA for critical bus masters
- Second layer : RR for non-critical bus masters



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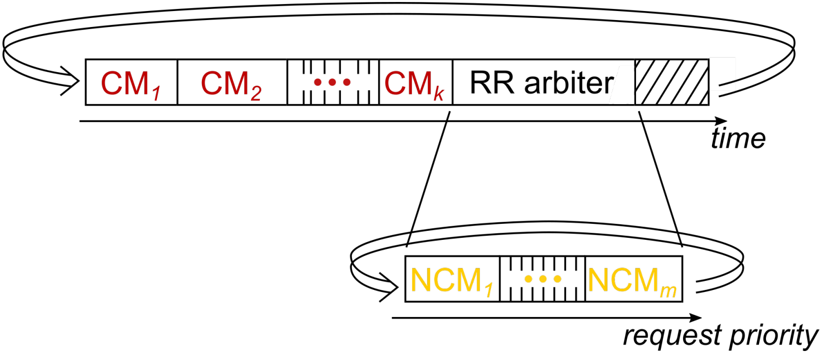


Criticality- and Requirement-Aware Bus Arbiter

- First layer : arbitration between criticality classes
- Second layer : arbitration between tasks of the elected criticality class

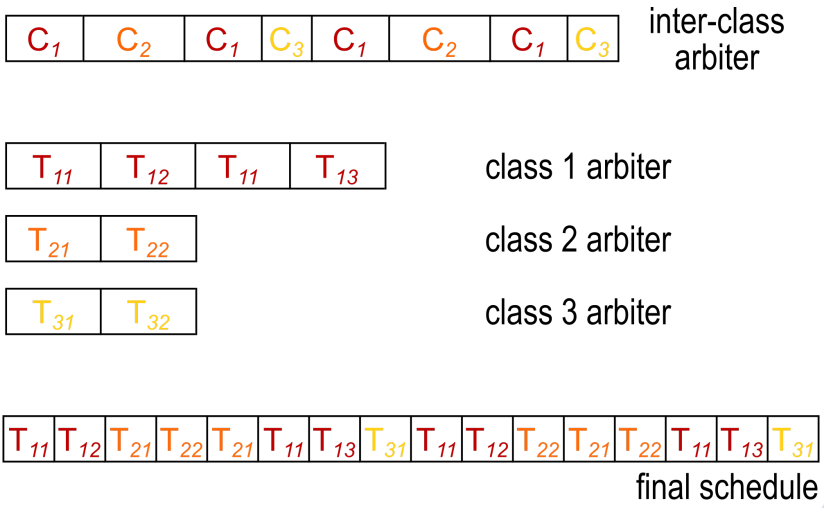
Criticality- and Requirement-Aware Bus Arbiter

- First layer : arbitration between criticality classes
- Second layer : arbitration between tasks of the elected criticality class
- Both layers are Weighted Harmonic RR

Weighted Harmonic Round Robin

- Bus control granted for 1 request only
- Each master can get several slots per period
- Slots are evenly distributed

CArb - Example



C_1 C_2 C_1 C_3 C_1 C_2 C_1 C_3
inter-class arbiter
T_{11} T_{12} T_{11} T_{13}
class 1 arbiter
T_{21} T_{22}
class 2 arbiter
T_{31} T_{32}
class 3 arbiter
T_{11} T_{12} T_{21} T_{22} T_{21} T_{11} T_{13} T_{31} T_{11} T_{12} T_{22} T_{21} T_{22} T_{11} T_{13} T_{31}
final schedule

CArb - Arbiter-level Mode Switch

$\mathrm{WCET}_{\mathit{total}}(\mathrm{T}_{\mathit{13}}) < \mathit{exec\_time}(\mathrm{T}_{\mathit{13}})$

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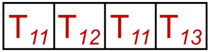
$\text{WCET}_{iso}(\text{T}_{13}) < exec\_time(\text{T}_{13}) < \text{WCET}_{total}(\text{T}_{13})$
$\rightarrow$ Cut interference, arbiter-level mode switch



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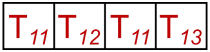
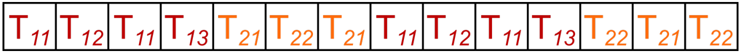
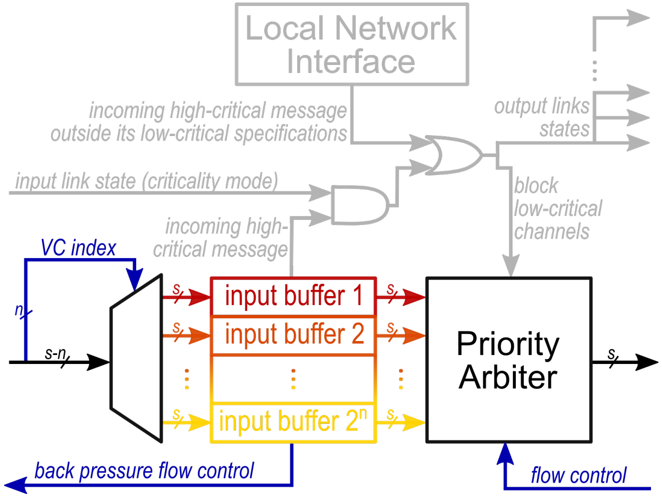


If $exec\_time(\text{T}_{13}) - \text{WCET}_{iso}(\text{T}_{13}) < threshold$
$\rightarrow$ Cut only part of the interference



Resource Management for Mixed-Criticality Systems

Wormhole Protocol for Mixed-Criticality



Local Network Interface
incoming high-critical message outside its low-critical specifications
input link state (criticality mode)
output links states
block low-critical channels
incoming high-critical message
VC index
n
s-n
s
input buffer 1
input buffer 2
input buffer 2^n
Priority Arbiter
back pressure flow control
flow control

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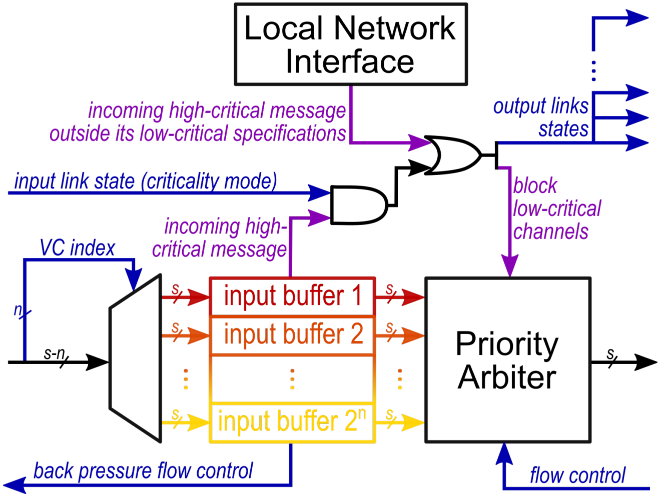
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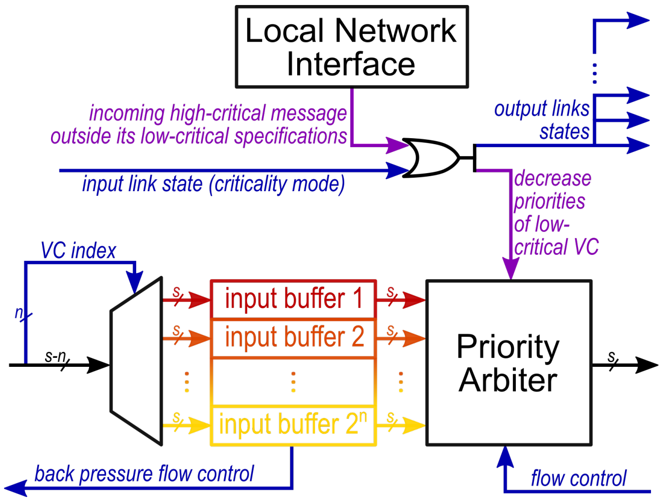
WPMC-Flood


Local Network Interface
incoming high-critical message outside its low-critical specifications
input link state (criticality mode)
output links states
decrease priorities of low-critical VC
VC index
n
s-n
s
input buffer 1
input buffer 2
⋮
input buffer 2ⁿ
Priority Arbiter
back pressure flow control
flow control

Wormhole with Blocking Counter

The header flit of critical messages contains a *Blocking Counter* field.

<u>Network Interface</u>

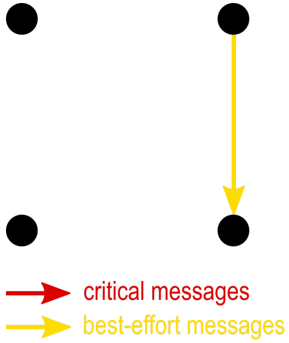
```
initialize BC value

(with maximum
number of times
the message can
be delayed)
```

<u>Router</u>

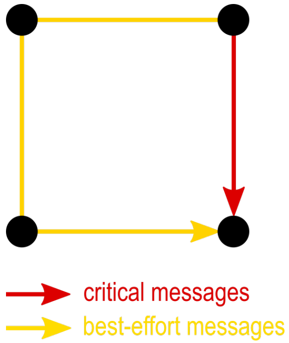
```
if message is stalled
    decrement BC
    if BC = 0
        prioritize message
    end if
end if
```

Adaptive Routing



- Message BE1
  Path list : {(1,2), (2,2)}, {(1,2), (1,1), (2,1), (2,2)}

Adaptive Routing



- Message BE1
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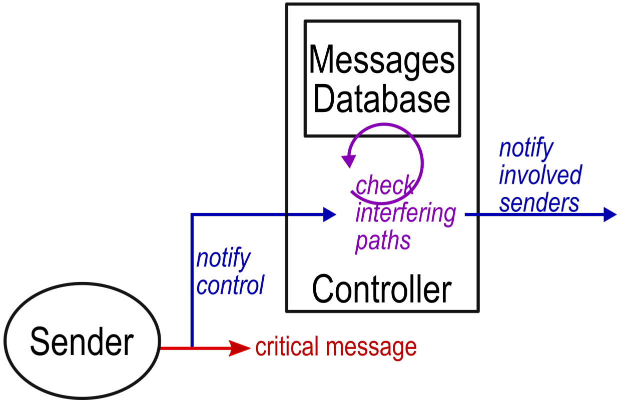
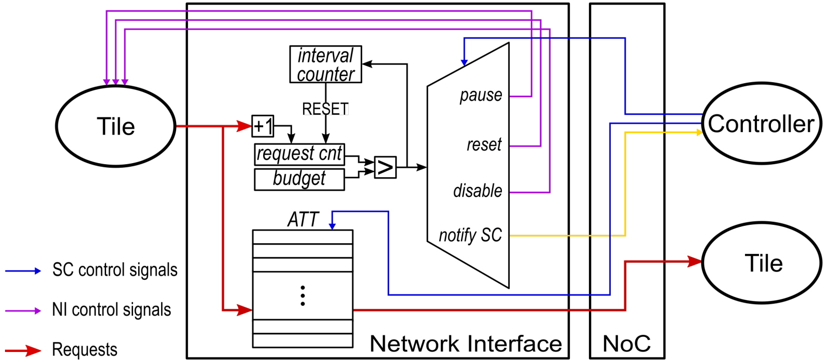
- Message C1
  Path list: {(1,2), (2,2)}

Adaptive Routing - Control Scheme



Resource Management for Mixed-Criticality Systems

Integrated Dependable Architecture for Many-Cores



Integrating Scheduling and Data mapping

Hardware model:

- 16 Clusters

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Hardware model:

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- Each SRAM bank has its own dedicated controller, which arbitrates between all cores and interfaces
  - NoC receiver interface always has priority
  - RR arbitration is performed between other components

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Software model:

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- Tasks of different criticality cannot be scheduled on the same time frame
- Joint computation of task schedule and data mapping to SRAM banks

Controlling interference from other tiles

When a task requires data to be fetched through the NoC

$$\begin{tikzcd}
\textit{Task A} \arrow[r] \arrow[d, "\textit{dependency constraint: delay t}"] & \textit{send request for data} \\
\textit{Task B} \arrow[r] & \textit{use data}
\end{tikzcd}$$

$t = 2 * \text{NoC worst-case latency} + \text{resource worst-case response time}$

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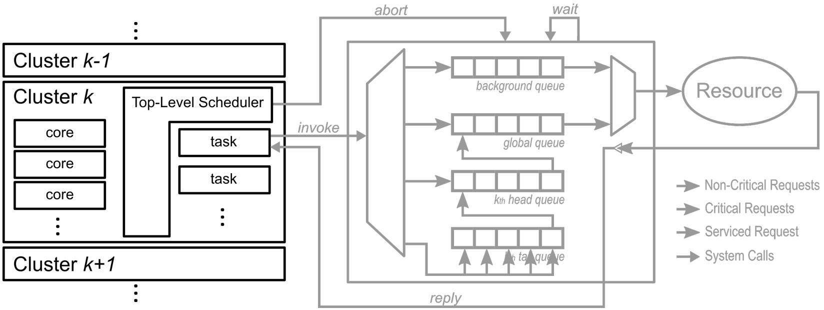
- For MCS, the IPC protocol should also take criticality into account

Resource Server for MCS



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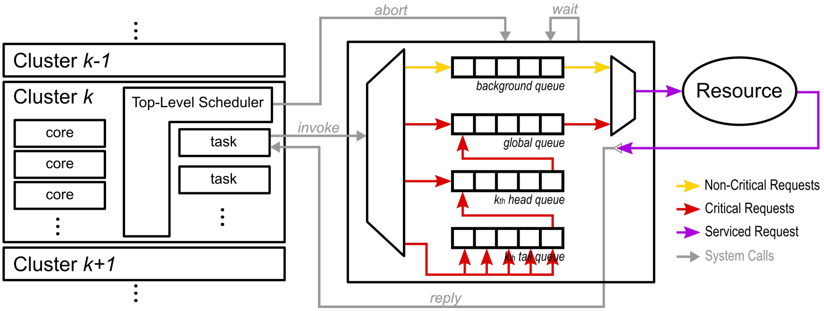

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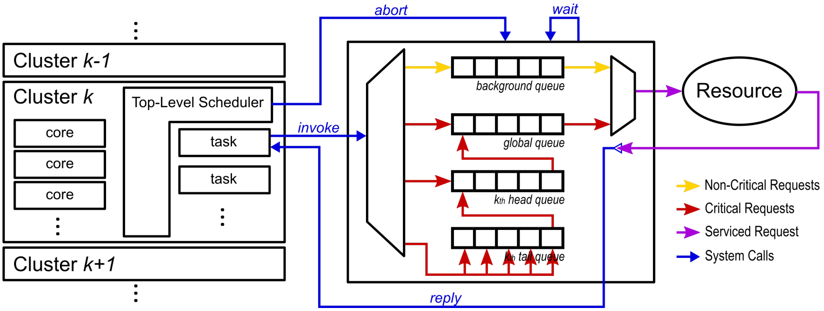

Resource Management for Mixed-Criticality Systems

Mixed Criticality Systems

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  - **Communication.**

¿ Questions ?