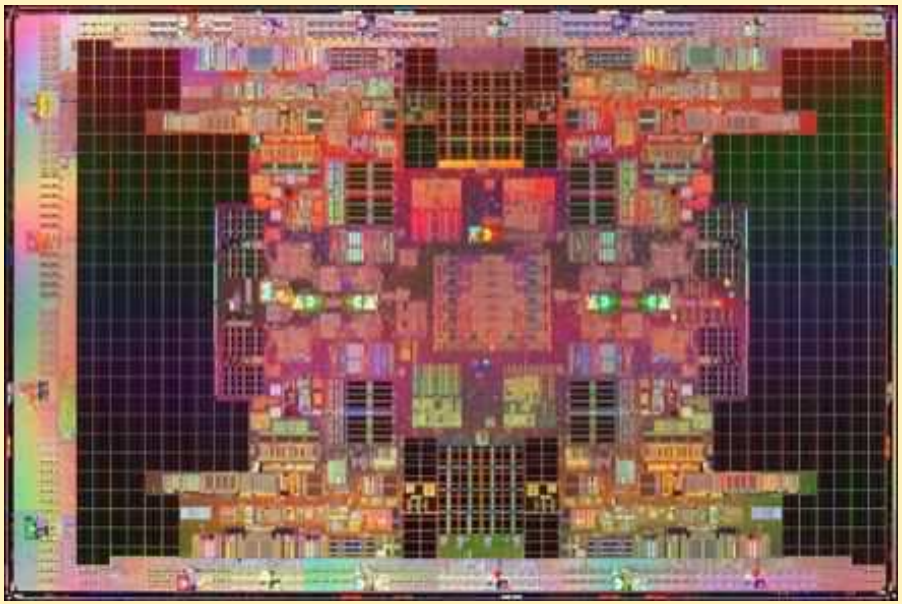
The Rise and Fall of System on Chip

Axel Jantsch

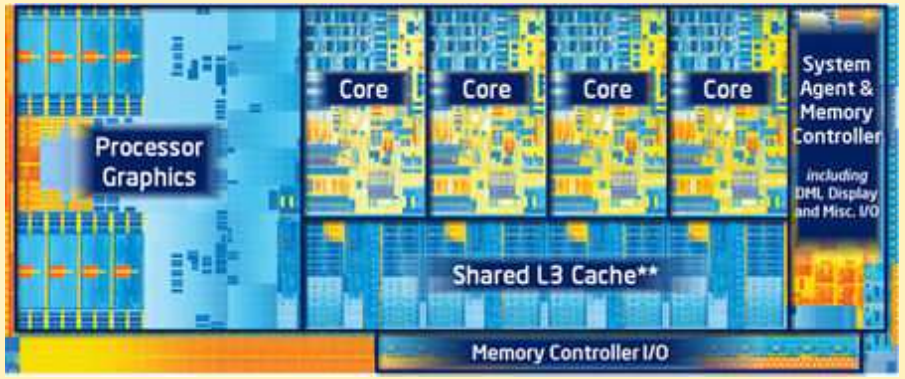
October 25, 2013

What is a System on Chip?

What is a SoC

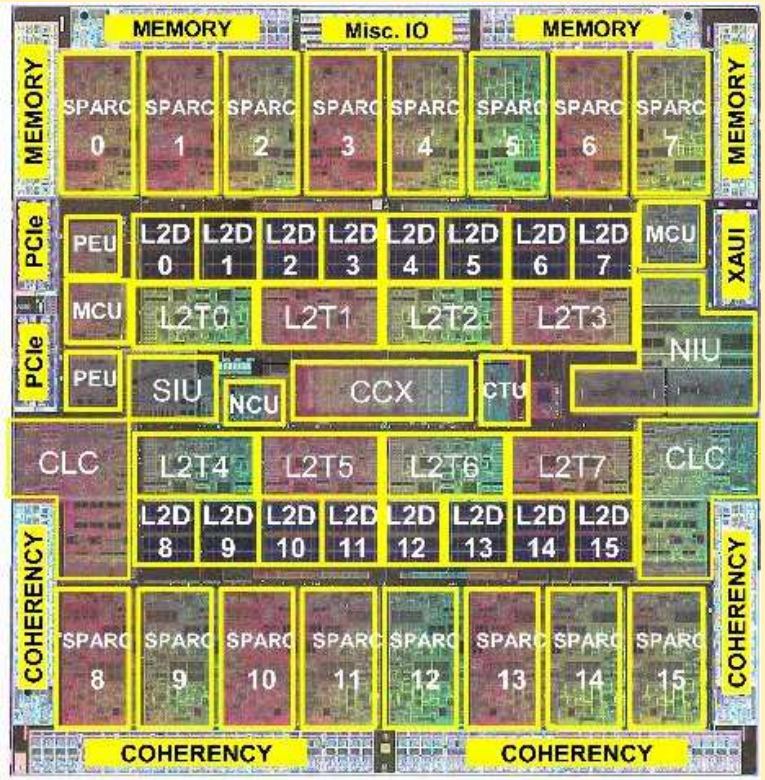


Intel Tukwila:
$2.046 \cdot 10^9$ Transistors
$21.5 \times 32.5\text{mm}^2$ 65nm Technology,
170 W, 2GHz

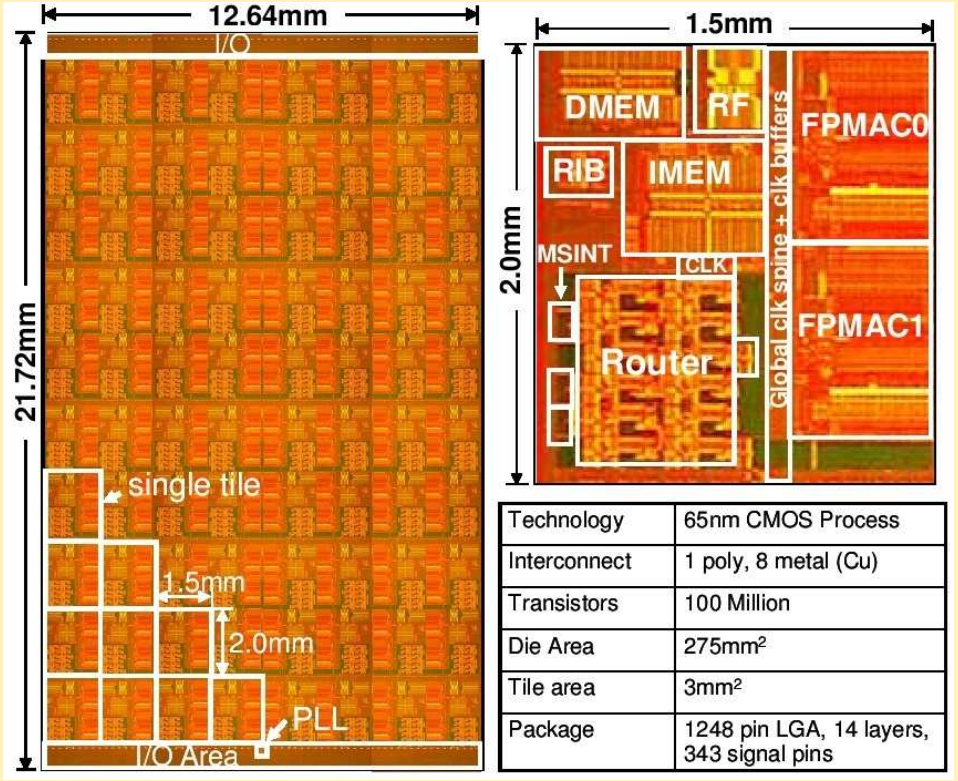


Intel Ivy Bridge:
$1.4 \cdot 10^9$ Transistors
160mm^2 22nm Technology,
77 W, 3.9 GHz

What is a SoC



Sun Niagara 3:
$1 \cdot 10^9$ Transistors
16 cores, 377mm^2 40nm Technology
1.67 GHz, 60 W



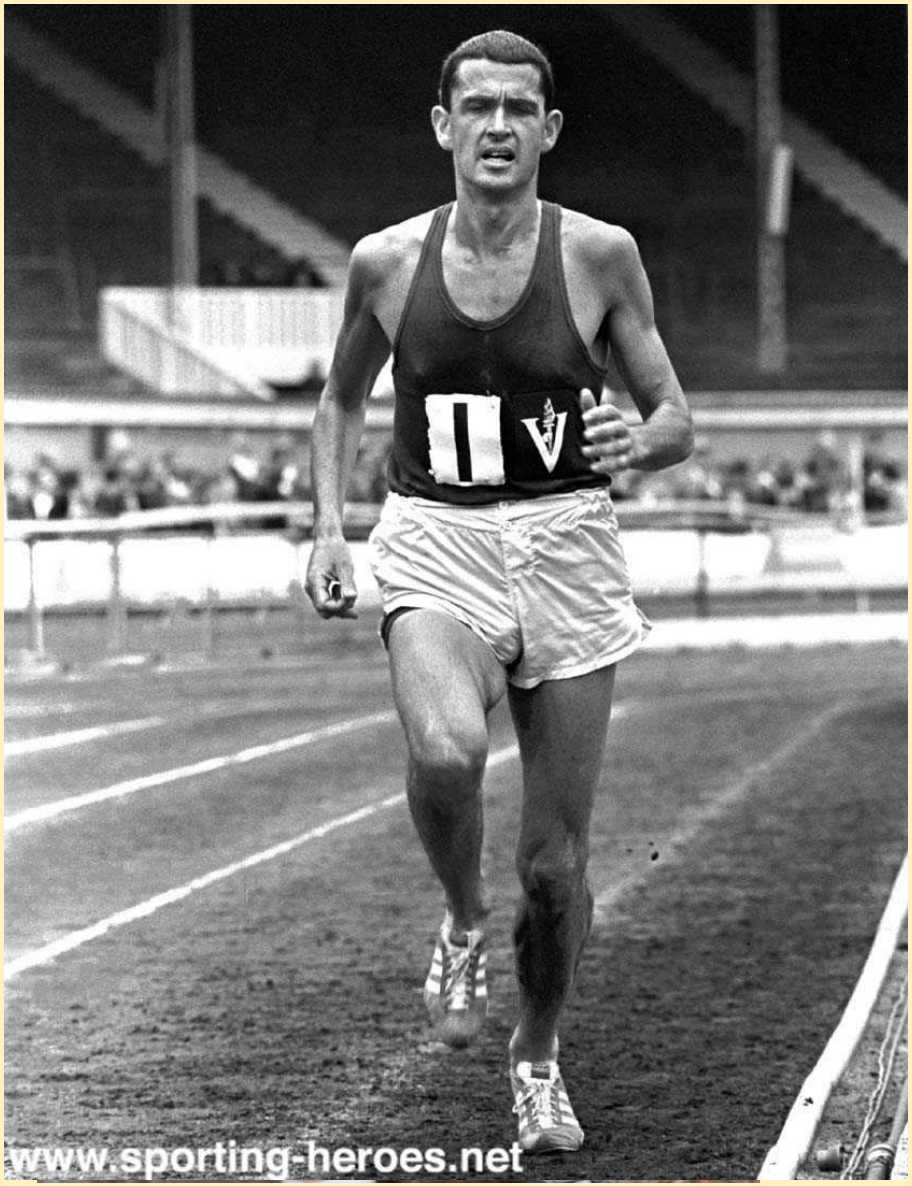
Technology	65nm CMOS Process
Interconnect	1 poly, 8 metal (Cu)
Transistors	100 Million
Die Area	275mm²
Tile area	3mm²
Package	1248 pin LGA, 14 layers, 343 signal pins

Intel Teraflop:
$100 \cdot 10^6$ Transistors
80 cores, 275mm^2 65nm Technology
3.67 GHz, 62 W

Moore's Law

1965

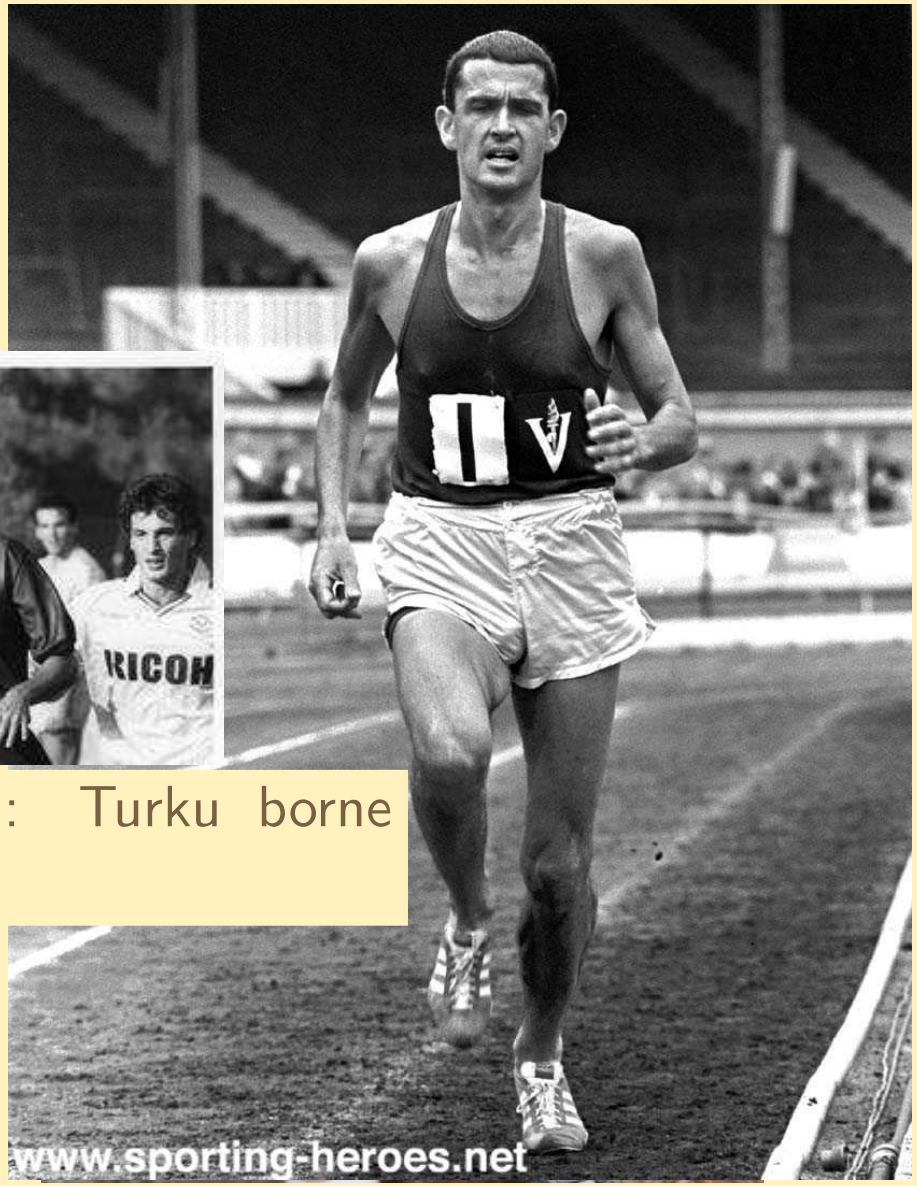
1965



Ron Clarke: 28:14.0 world record in 10 000 m

1965

Mika Aaltonen: Turku borne football player

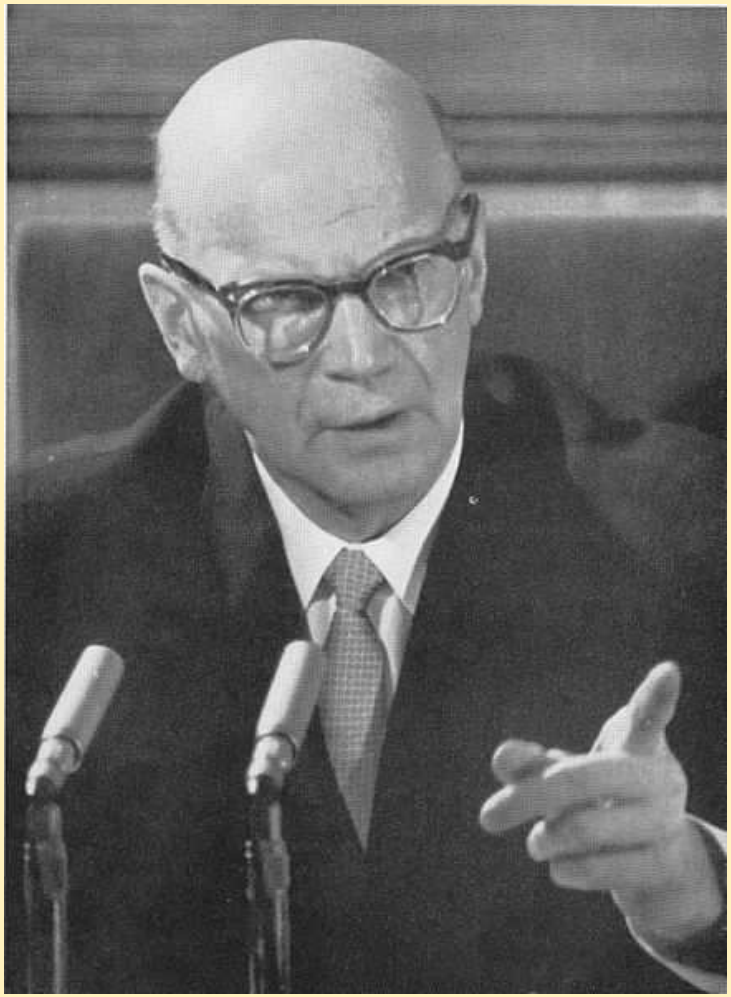


Ron Clarke: 28:14.0 world record in 10 000 m

1965

Rauno Aaltonen: Won European and Finish Rally Championship

1965

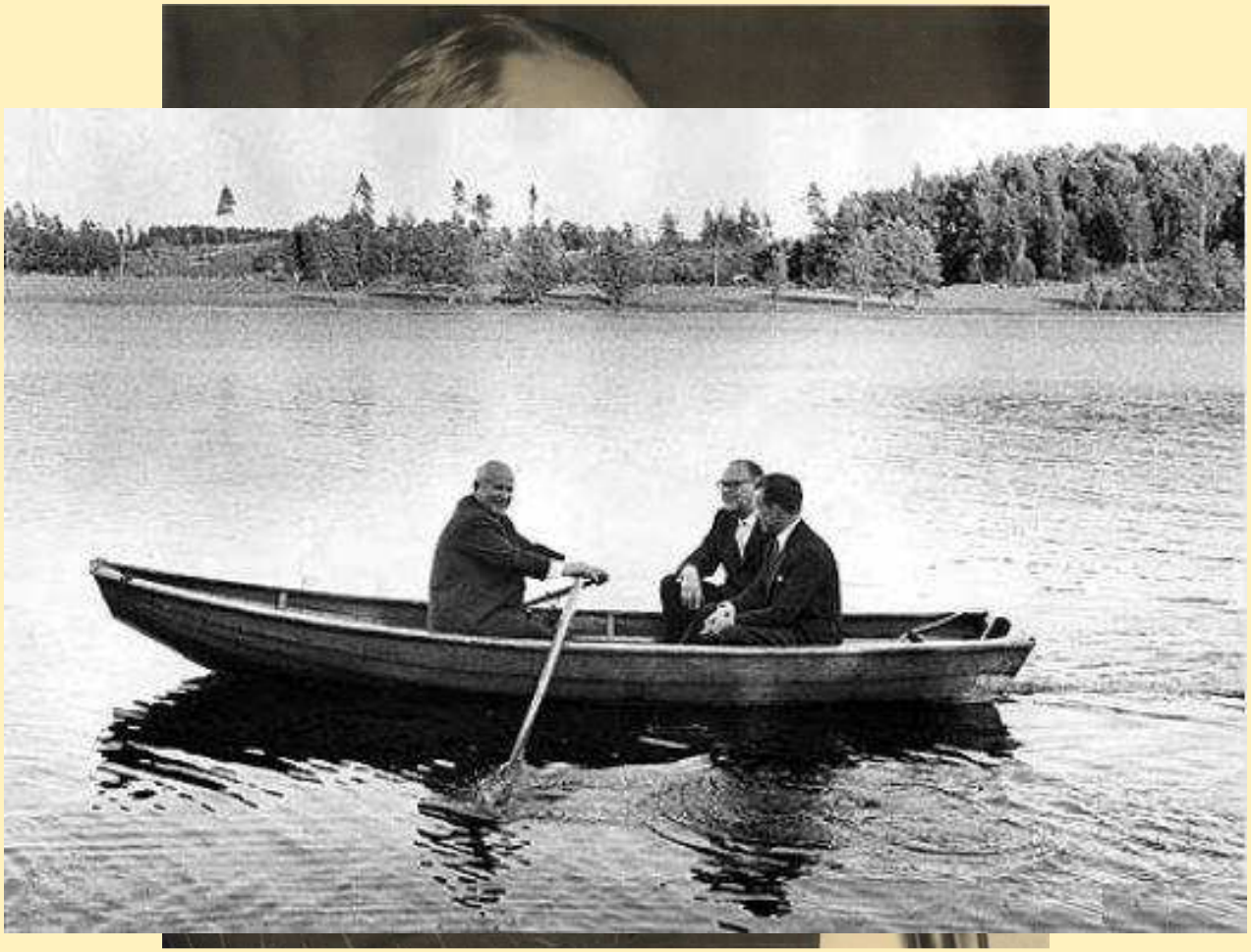


Urho Kekkonen: President 1956-82

1965

Tage Erlander: Prime Minister 1946-69

1965



Tage Erlander and Nikita Khrushchev

Tage Erlander: Prime Minister 1946-69

1965

Lyndon B. Johnson: US President 1963-1968

1965

Lyndon B. Johnson signing the immigration bill

1965

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1965

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1965

1965

1965

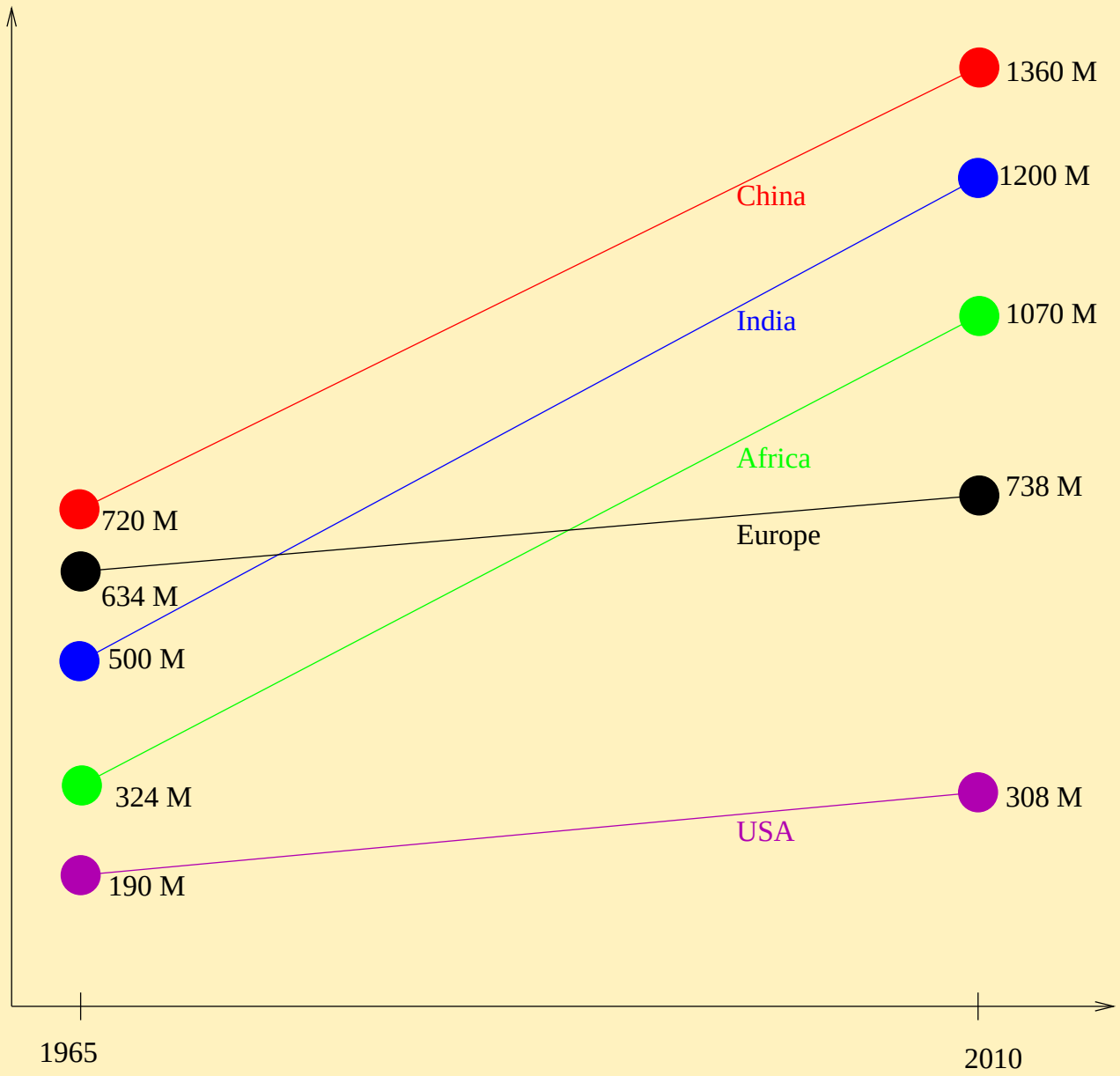
Great Leap: 1958-61; Cultural Revolution: 1966-76

1965

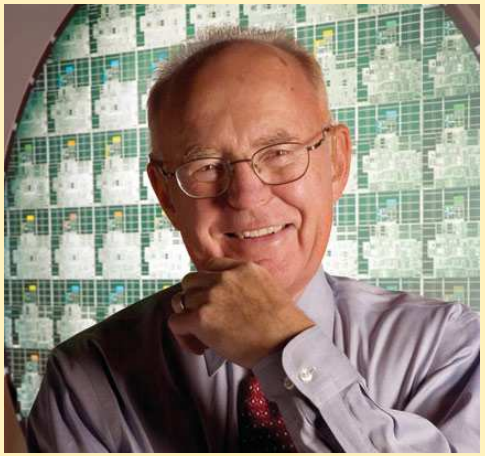
Grea 76

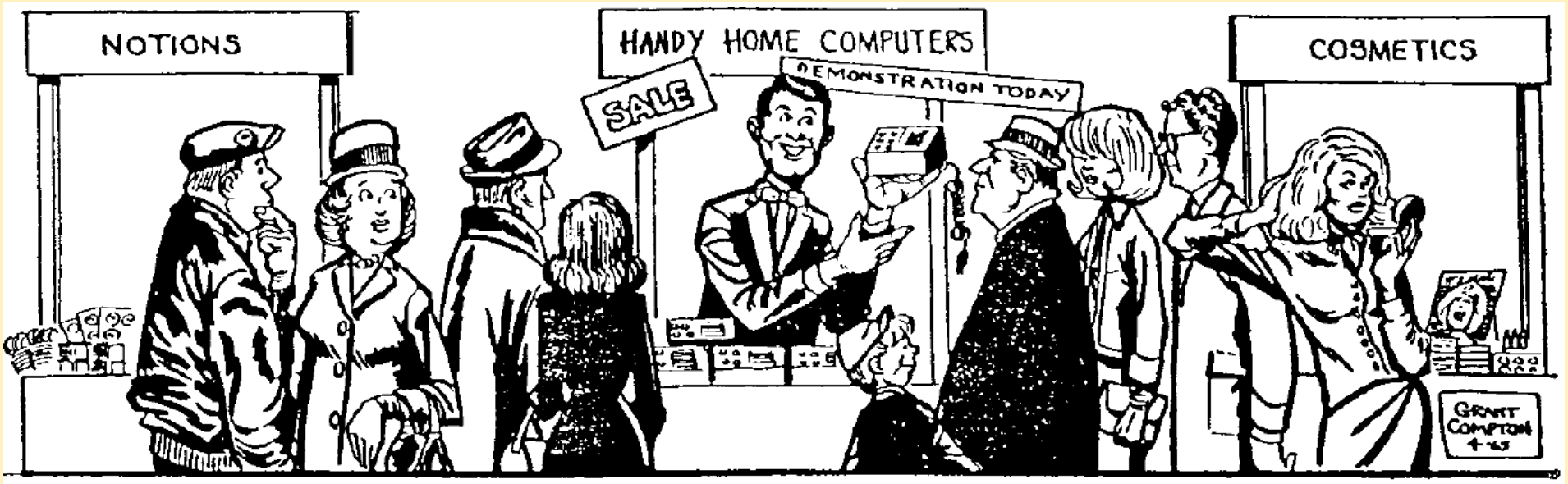
1965

1965


1360 M
1200 M
1070 M
738 M
308 M
China
India
Africa
Europe
USA
720 M
634 M
500 M
324 M
190 M
1965
2010

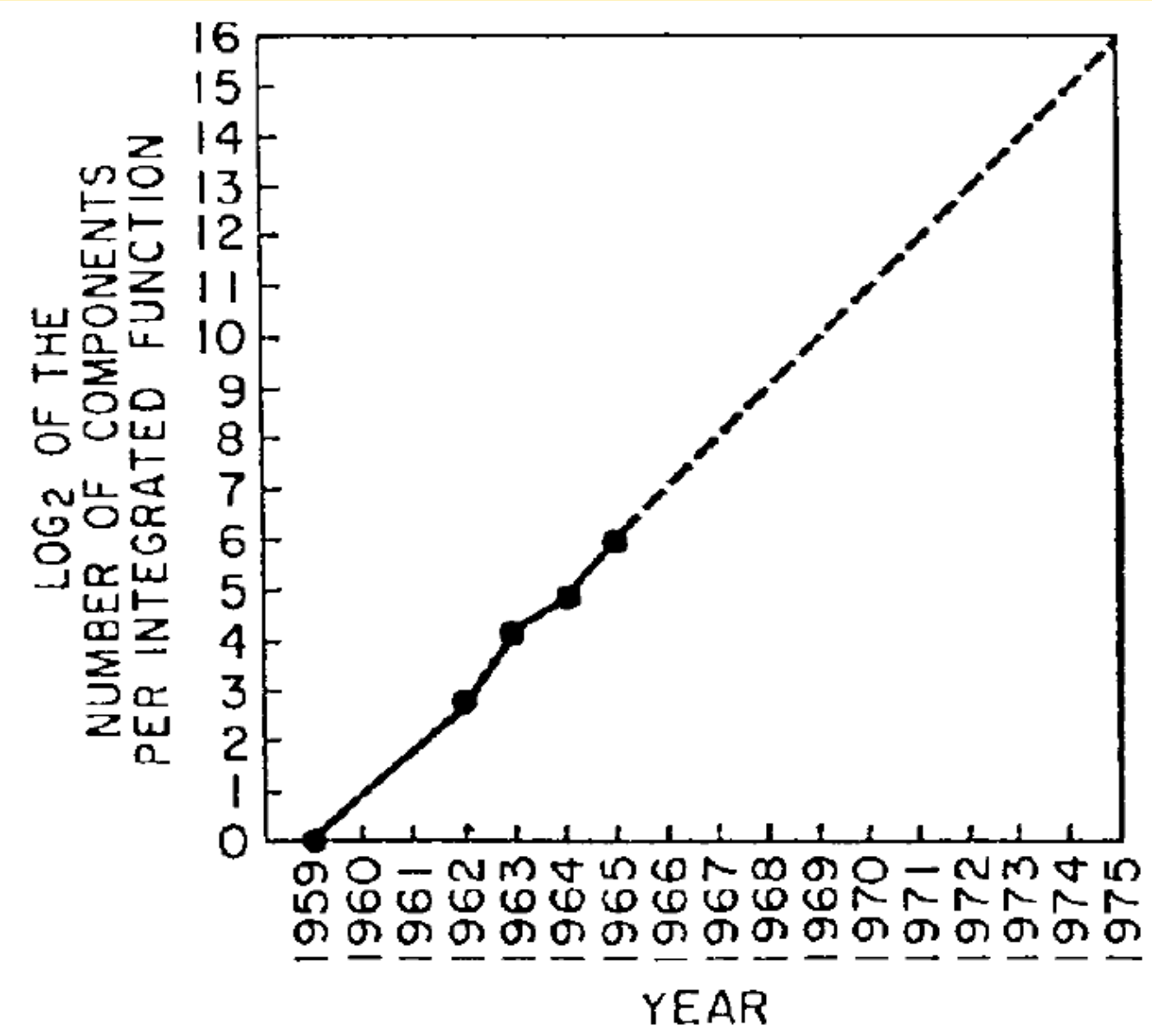
1965





Gordon E. Moore. "Cramming More Components onto Integrated Circuits". In: *Electronics* (1965), pp. 114–117

Moore's Law



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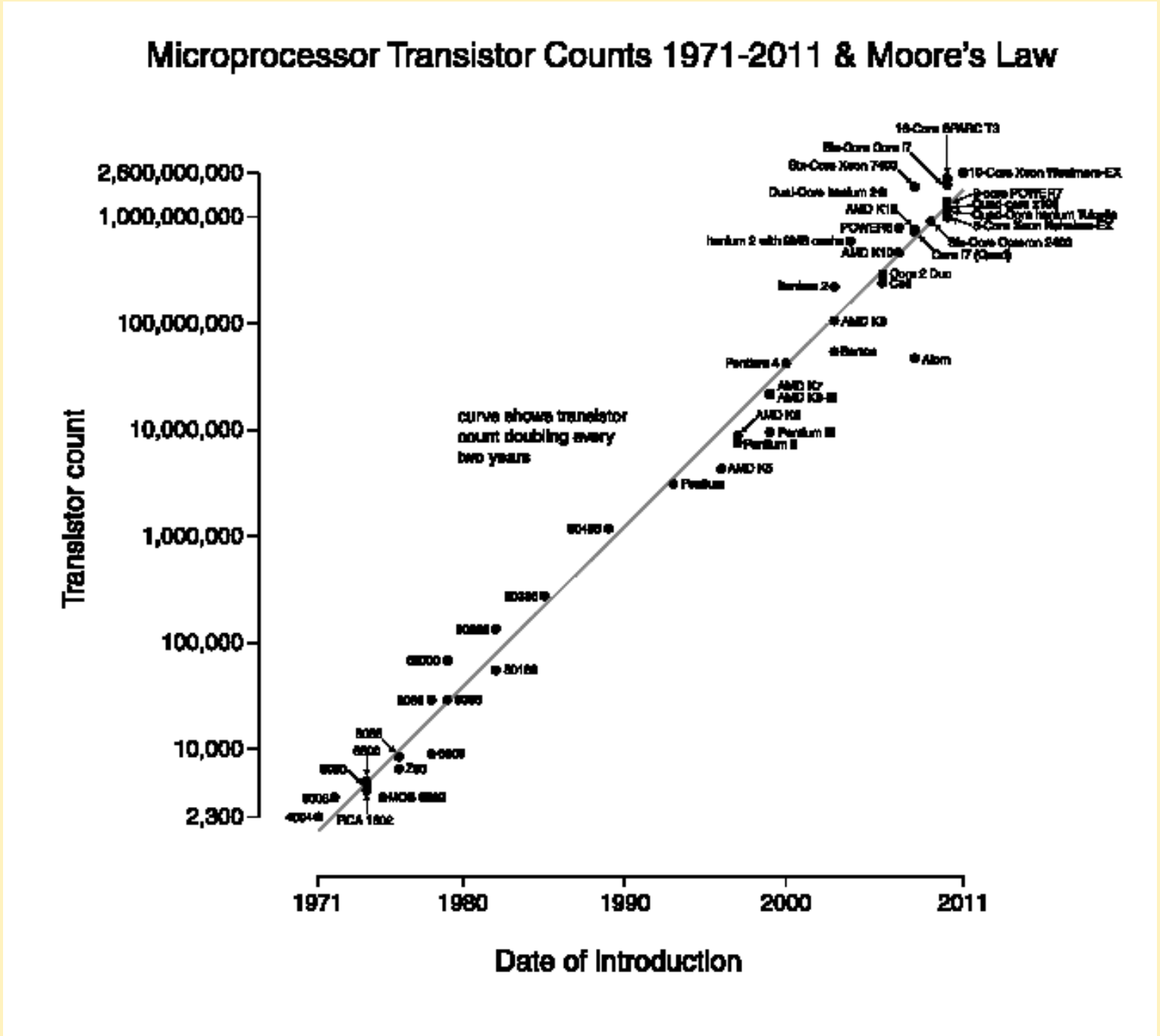
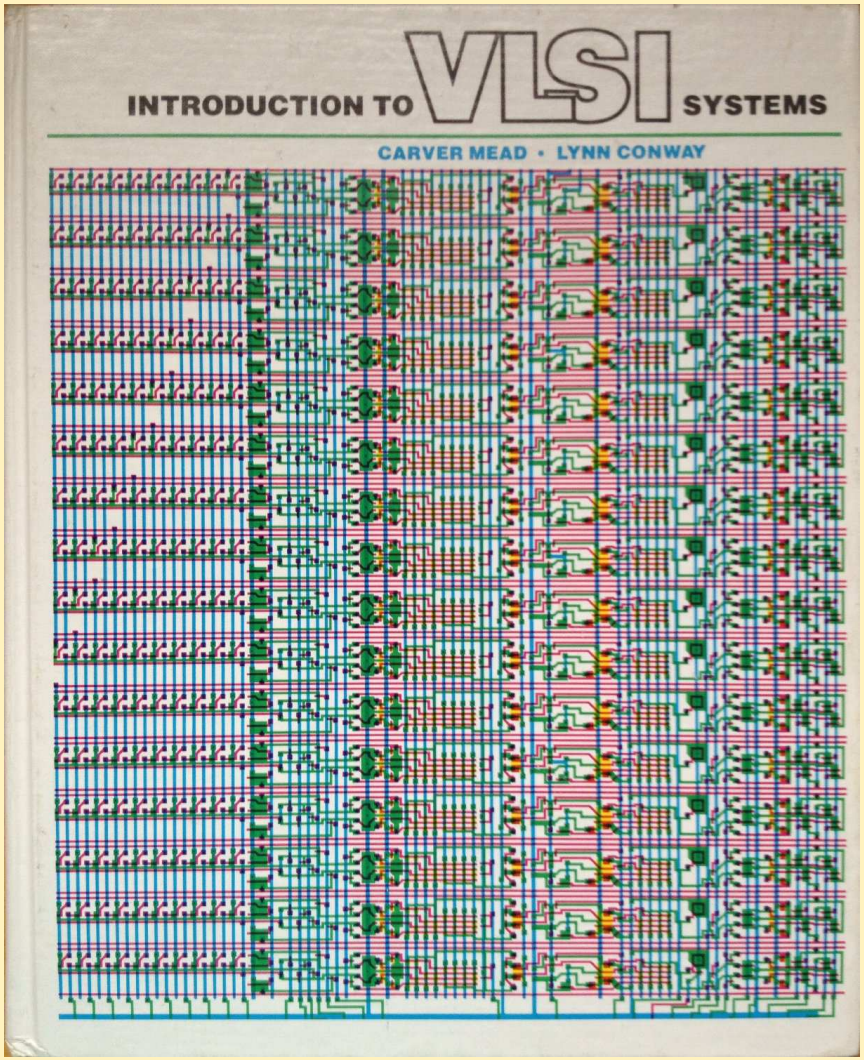

Microprocessor Transistor Counts 1971-2011 & Moore's Law
Transistor count
2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
curve shows transistor count doubling every two years
1971
1980
1990
2000
2011
Date of Introduction

Main Deflection Points

Mead-Conway Revolution

Carver Mead

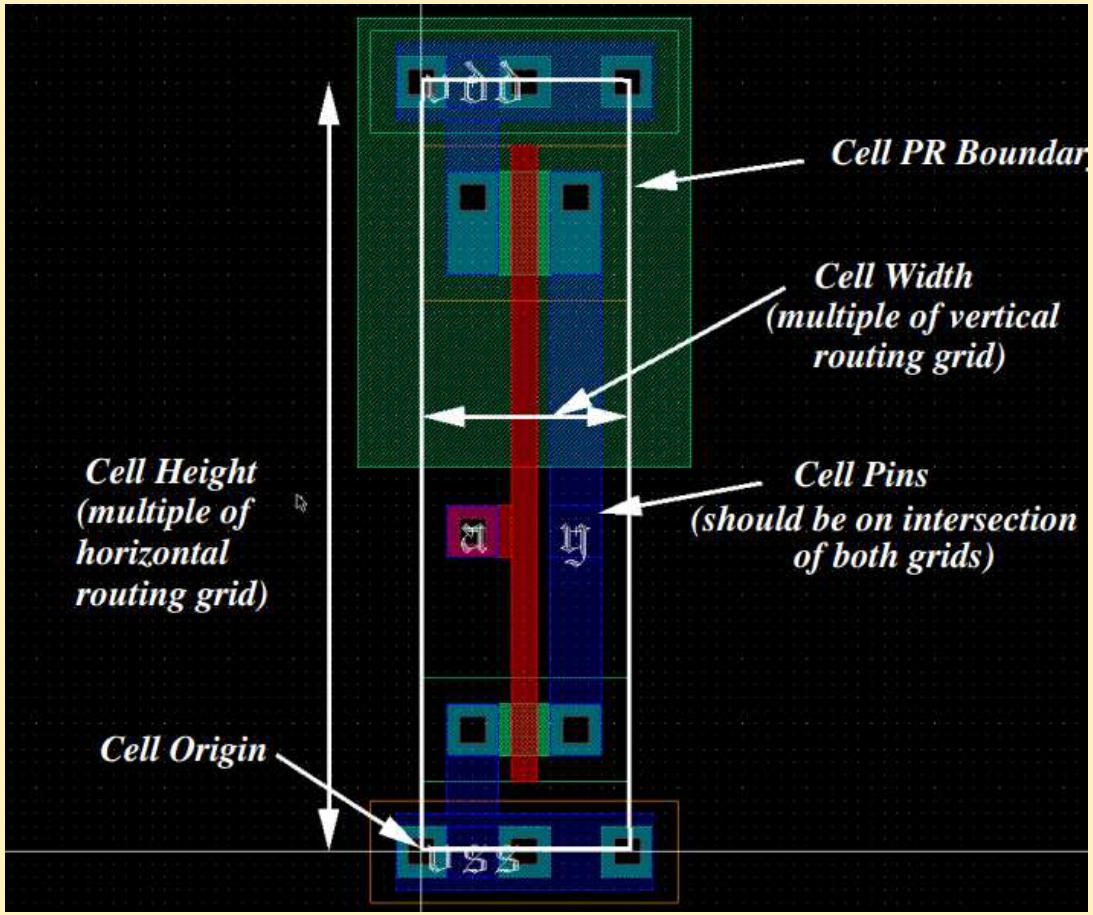


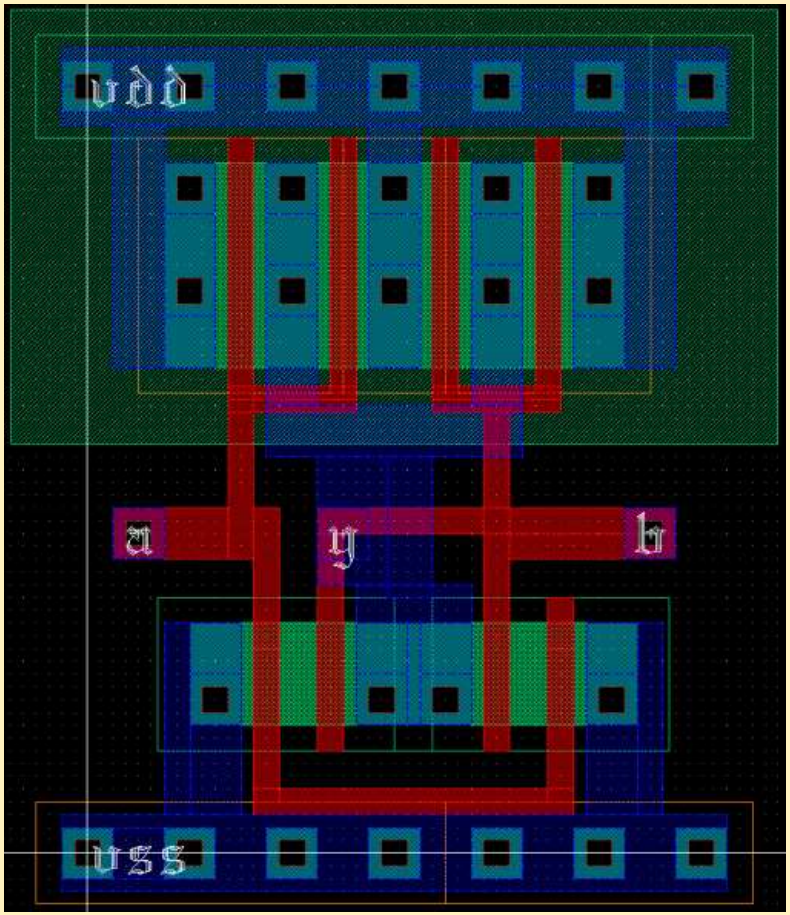
Lynn Conway

Carver Mead and Lynn Convay. *Introduction to VLSI Systems*. Addison-Wesley, 1980

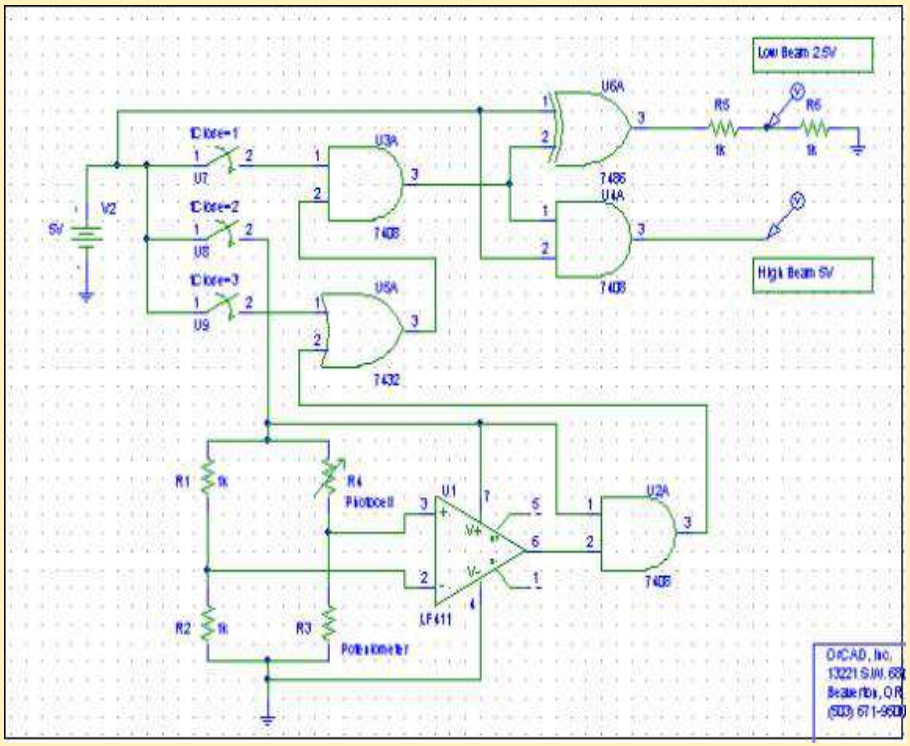
1980 - 20 000 Transistors

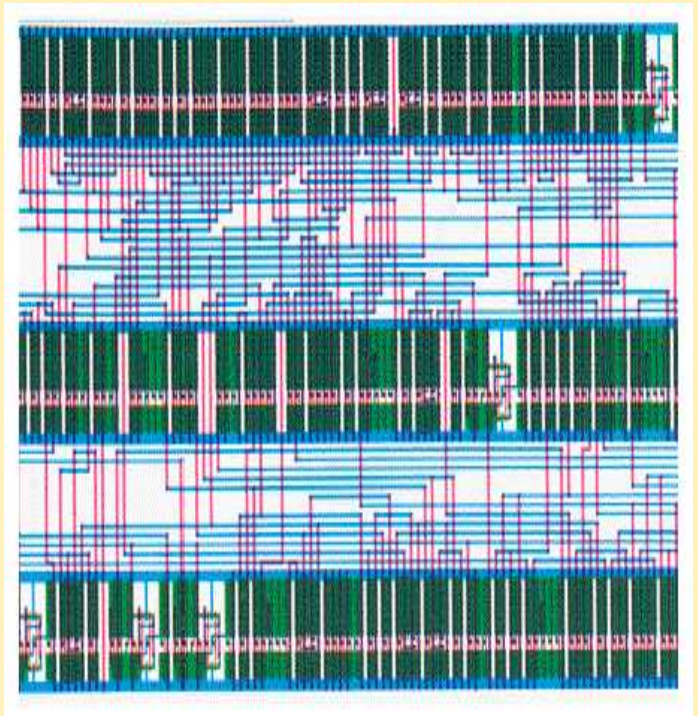
Standard Cells



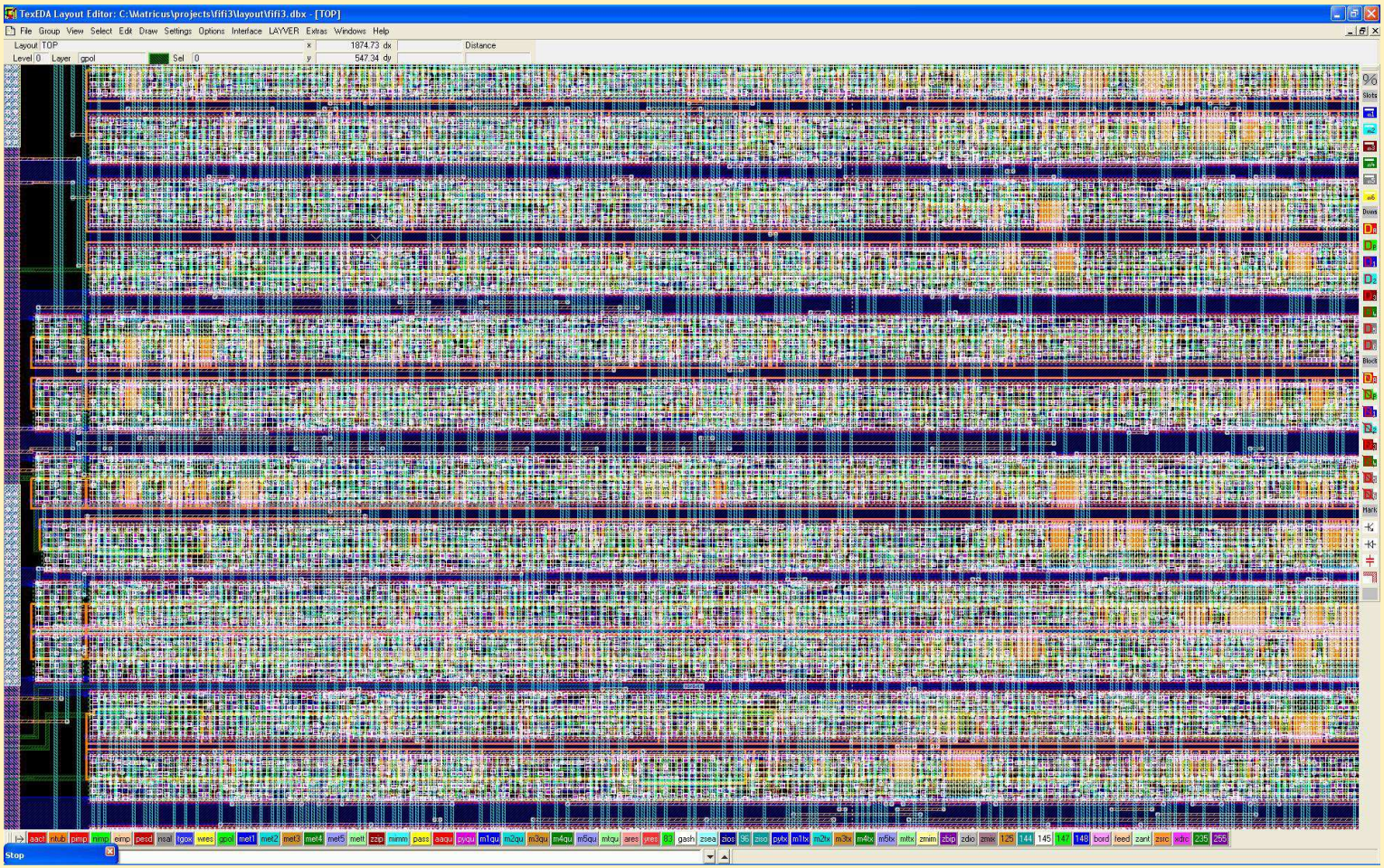


Standard Cells

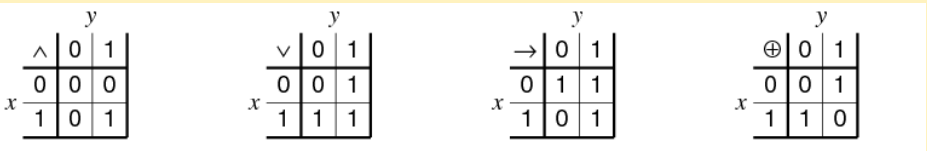




Standard Cells



Logic Synthesis



$\wedge$	0	1
0	0	0
1	0	1

$\vee$	0	1
0	0	1
1	1	1

$\rightarrow$	0	1
0	1	1
1	0	1

$\oplus$	0	1
0	0	1
1	1	0

Figure 1. Truth tables

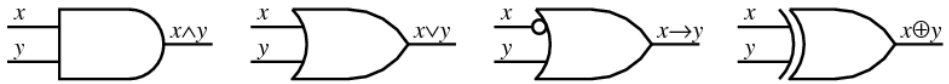


Figure 2. Logic gates

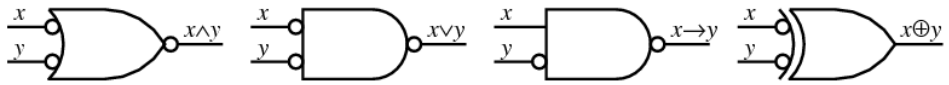
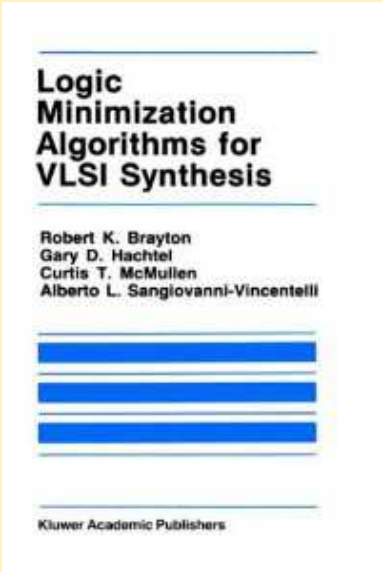


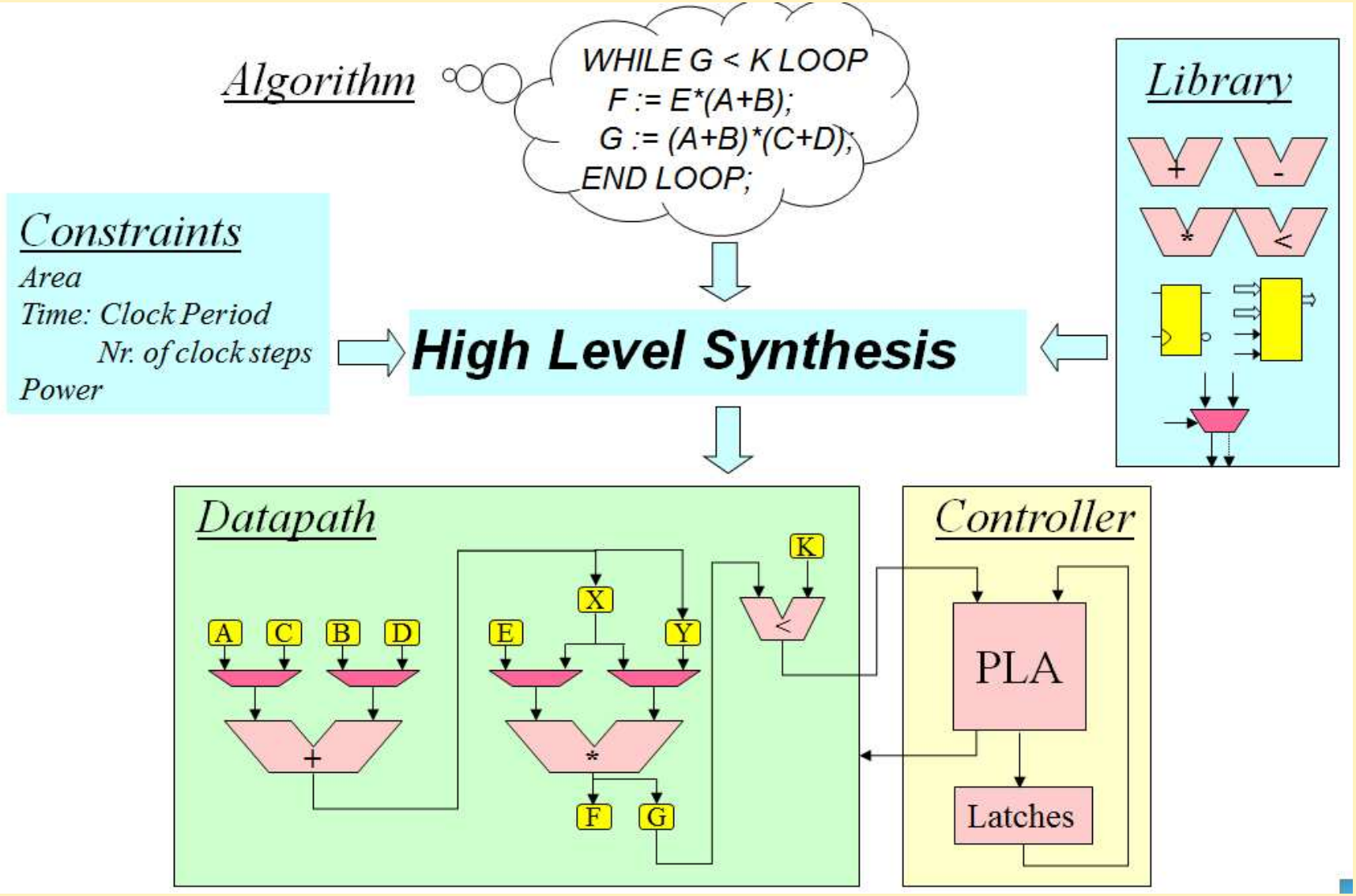
Figure 3. De Morgan equivalents

Figure 4. Venn diagrams



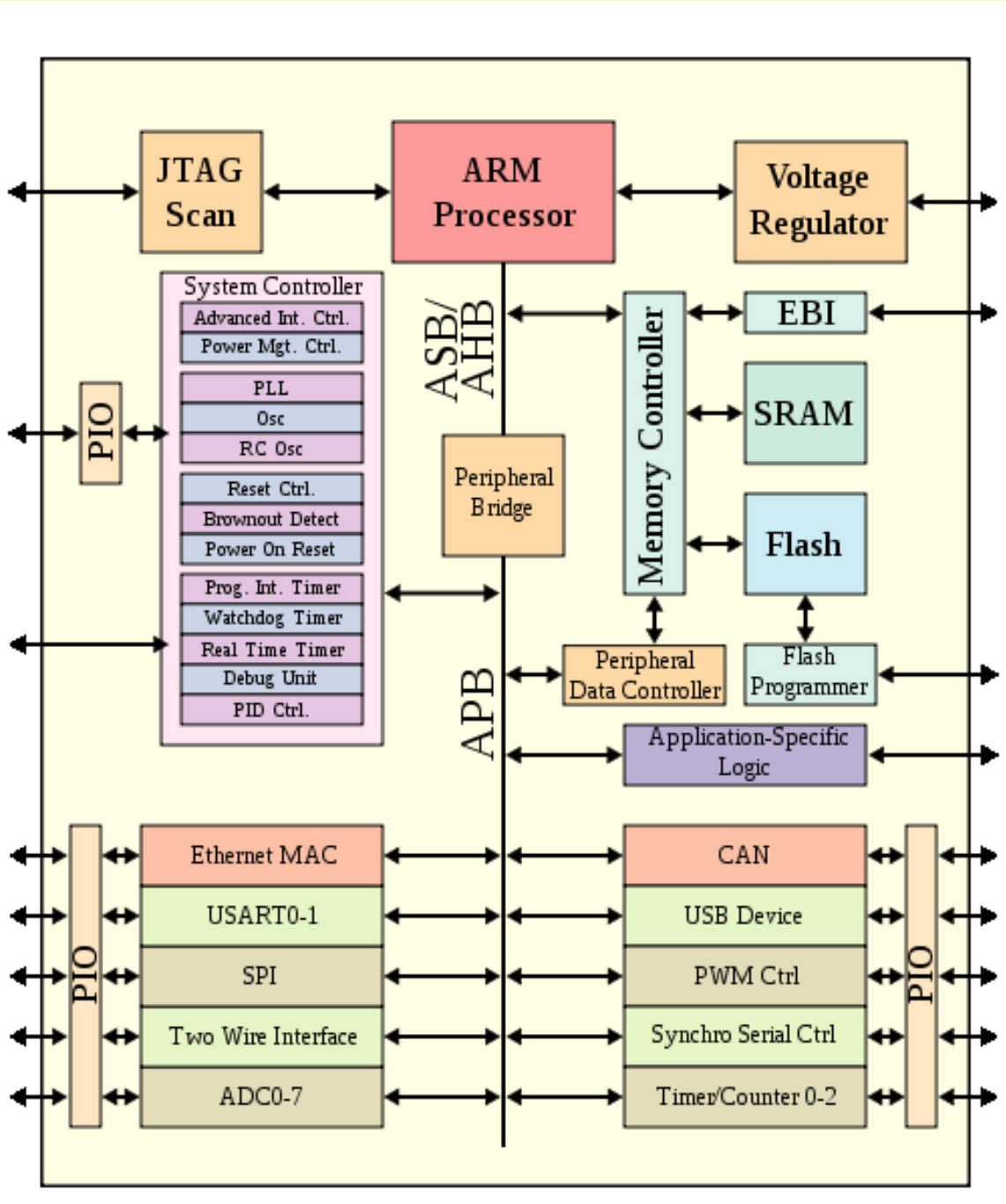
Robert K. Brayton, Gary D. Hachtel, Curtis T. McMullen, and Alberto L. Sangiovanni-Vincentelli. *Logic Minimization Algorithms for VLSI Synthesis*. Kluver Academic Publisher, 1984

High Level Synthesis

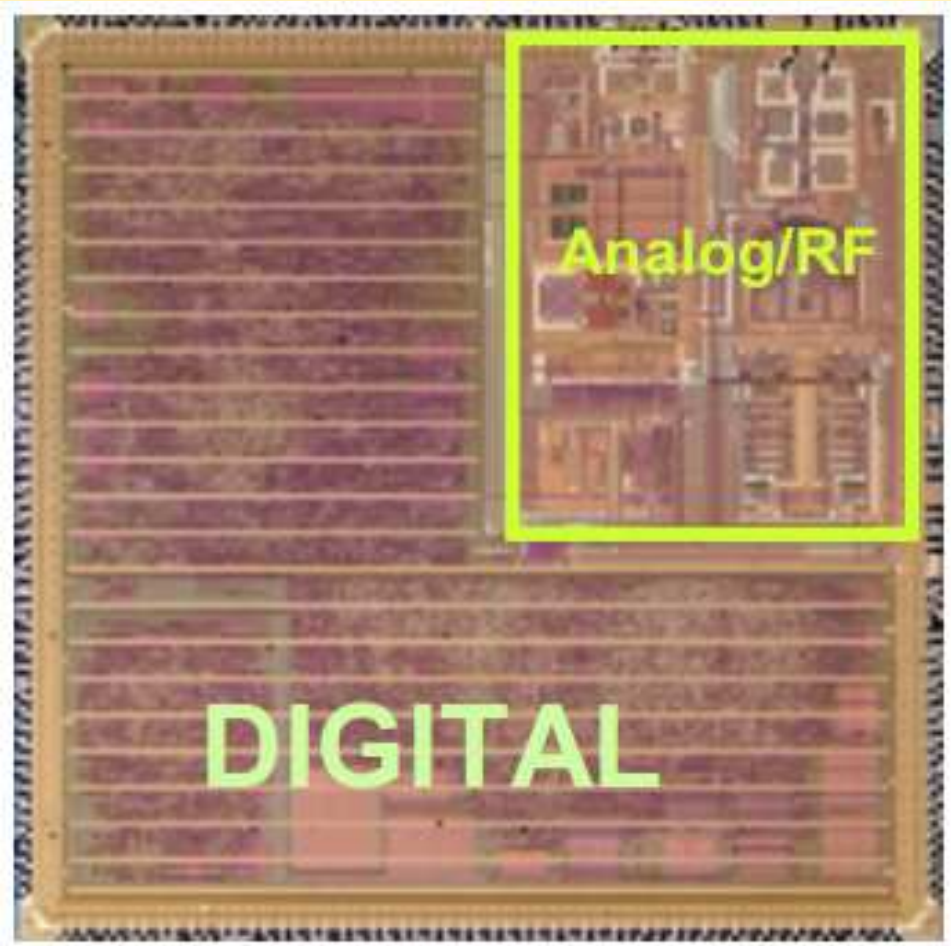


1990 - 1 000 000 Transistors

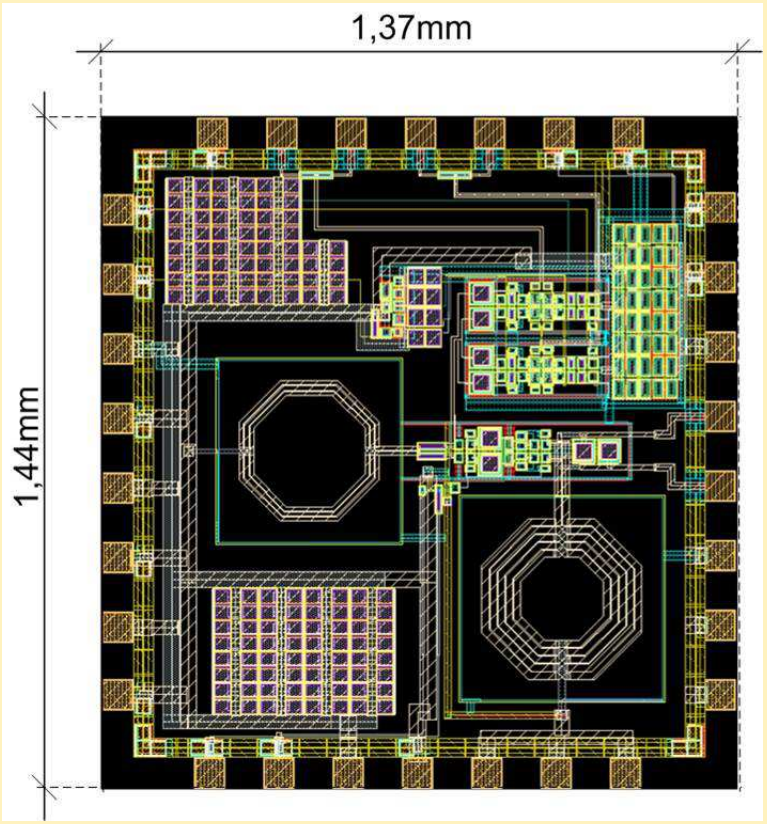
Emergence of SoC

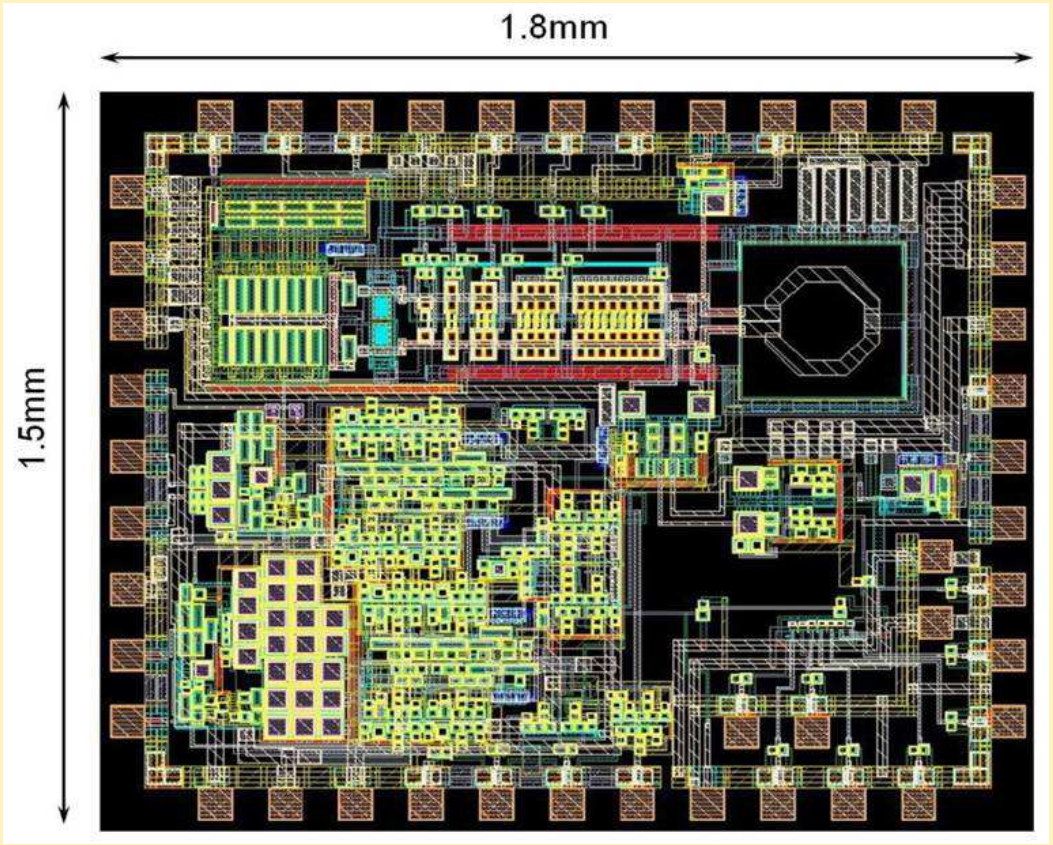


Emergence of SoC

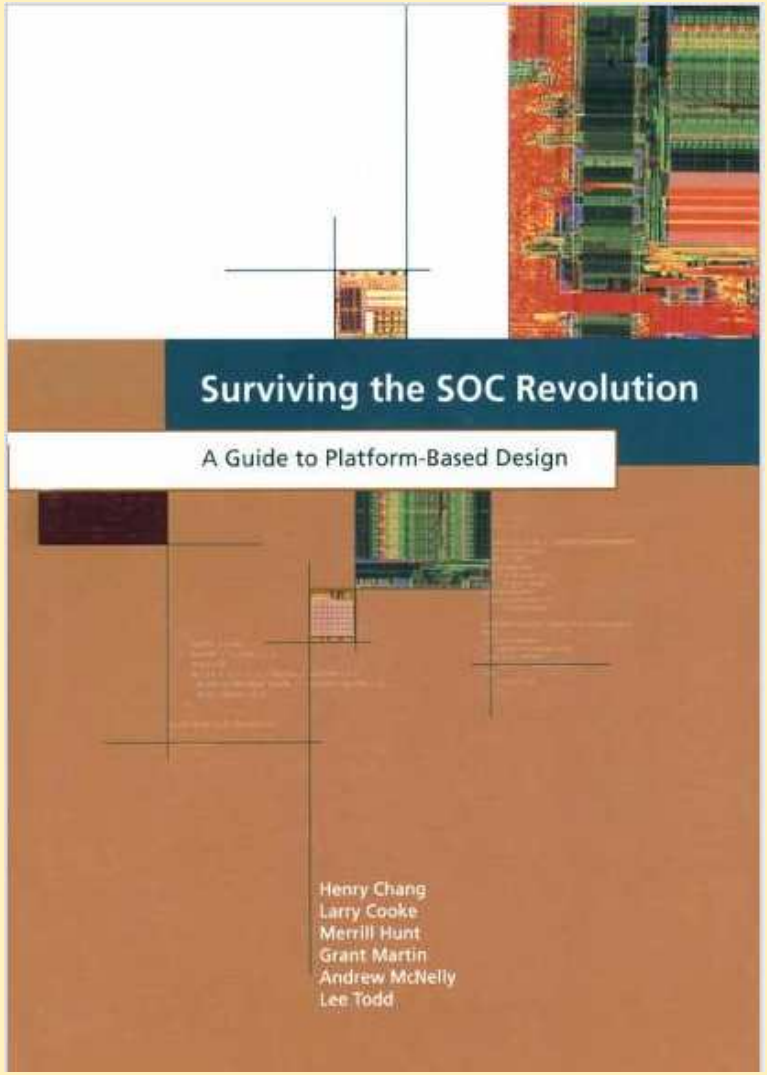


Emergence of SoC



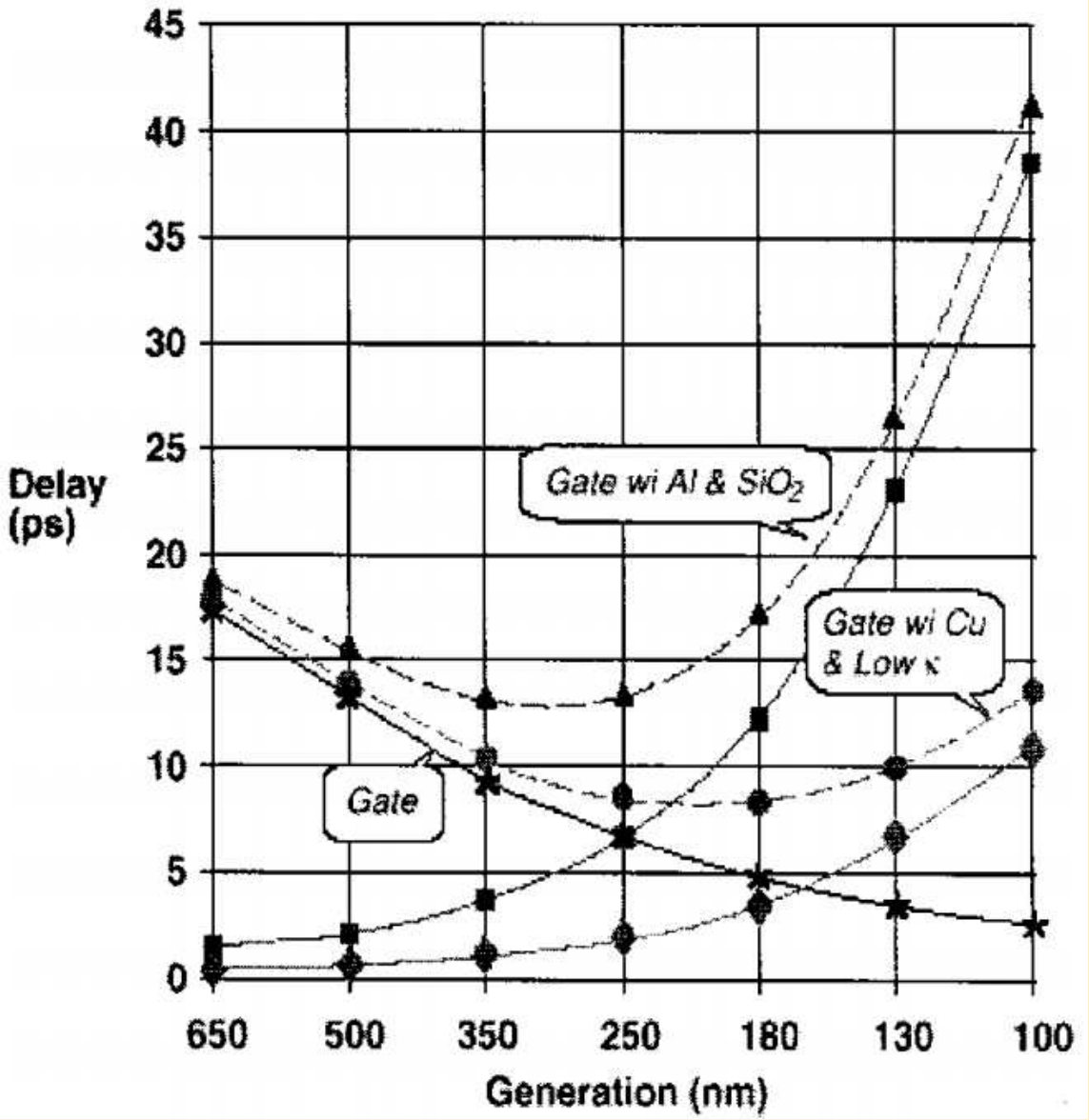


Emergence of SoC



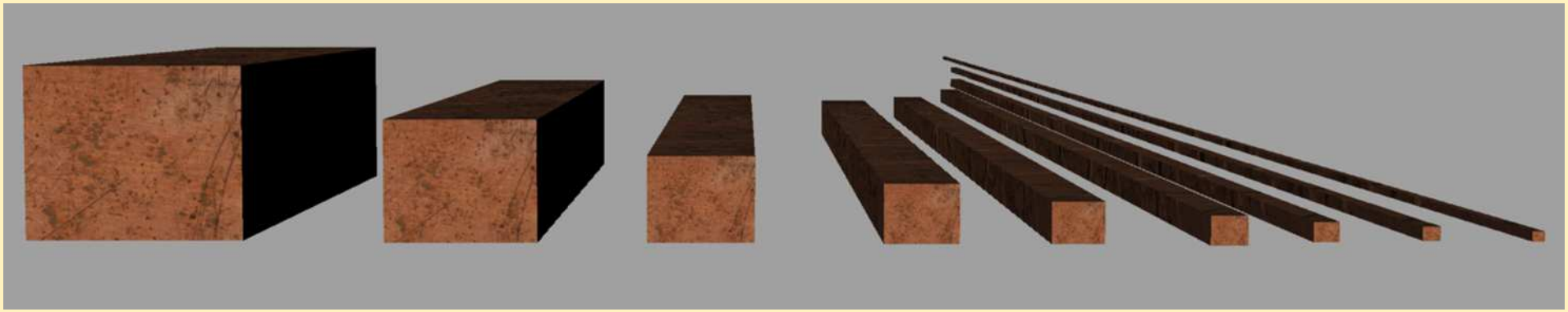
2000 - 20 000 000 Transistors

Wires Make Trouble



R. Ho, K.W. Mai, and M.A. Horowitz. "The future of wires". In: *Proceedings of the IEEE* 89.4 (2001), pp. 490–504

Wires Make Trouble



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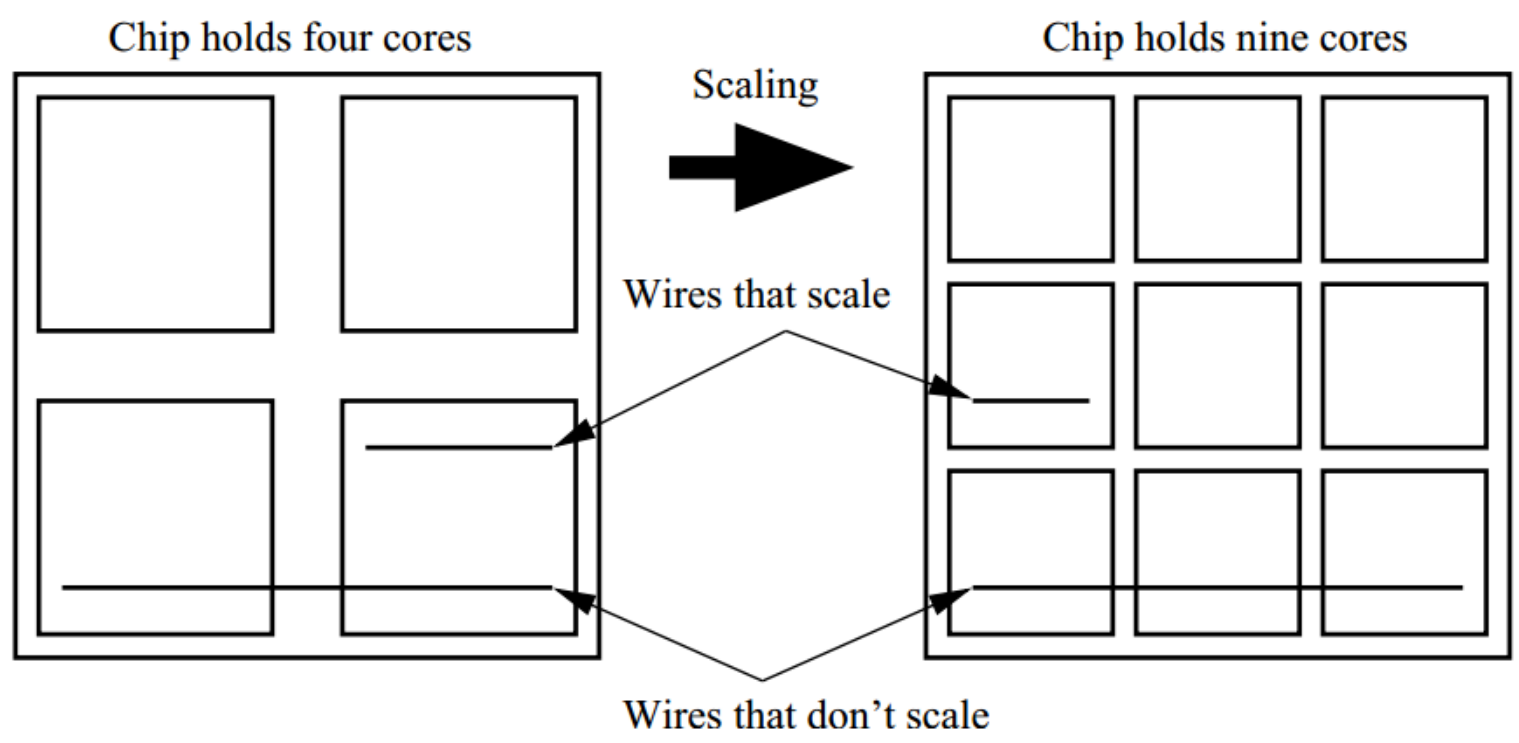

Ron Ho. "On-chip wires: Scaling and efficiency". PhD thesis. Stanford University, 2003

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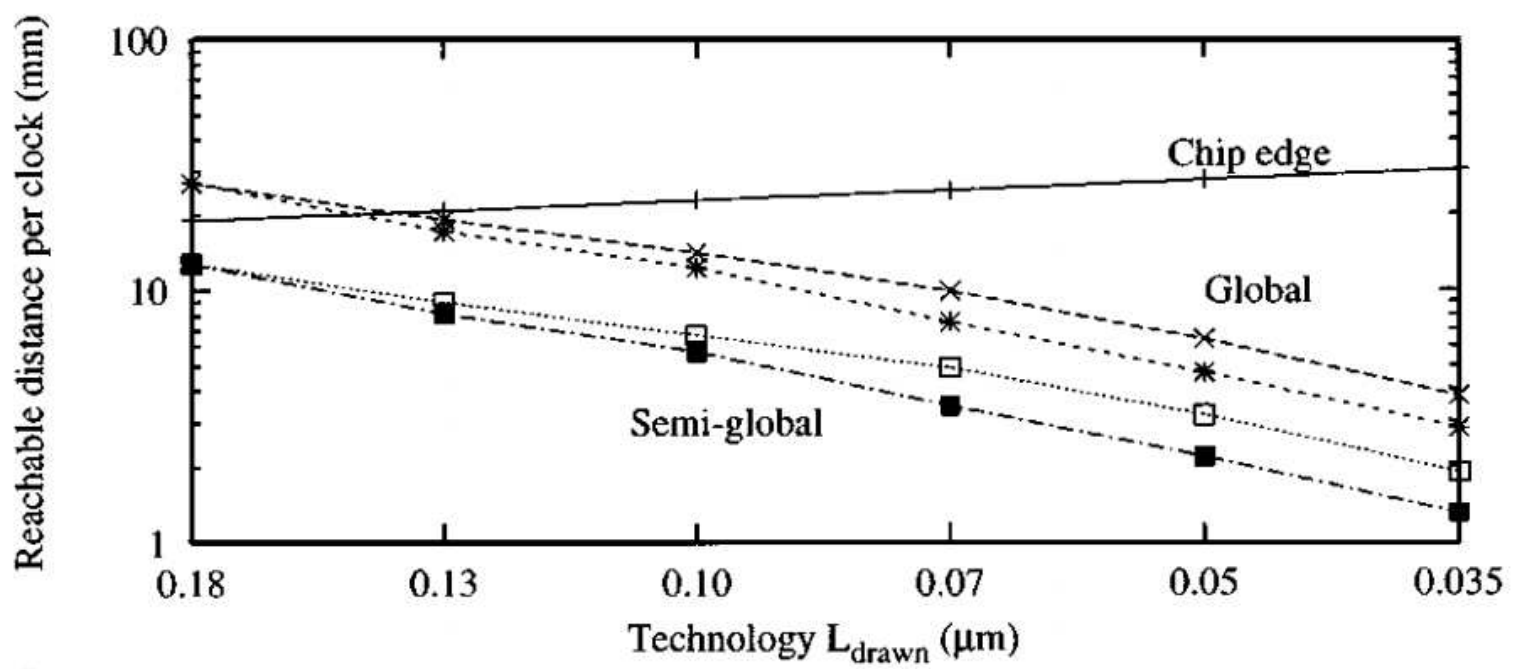

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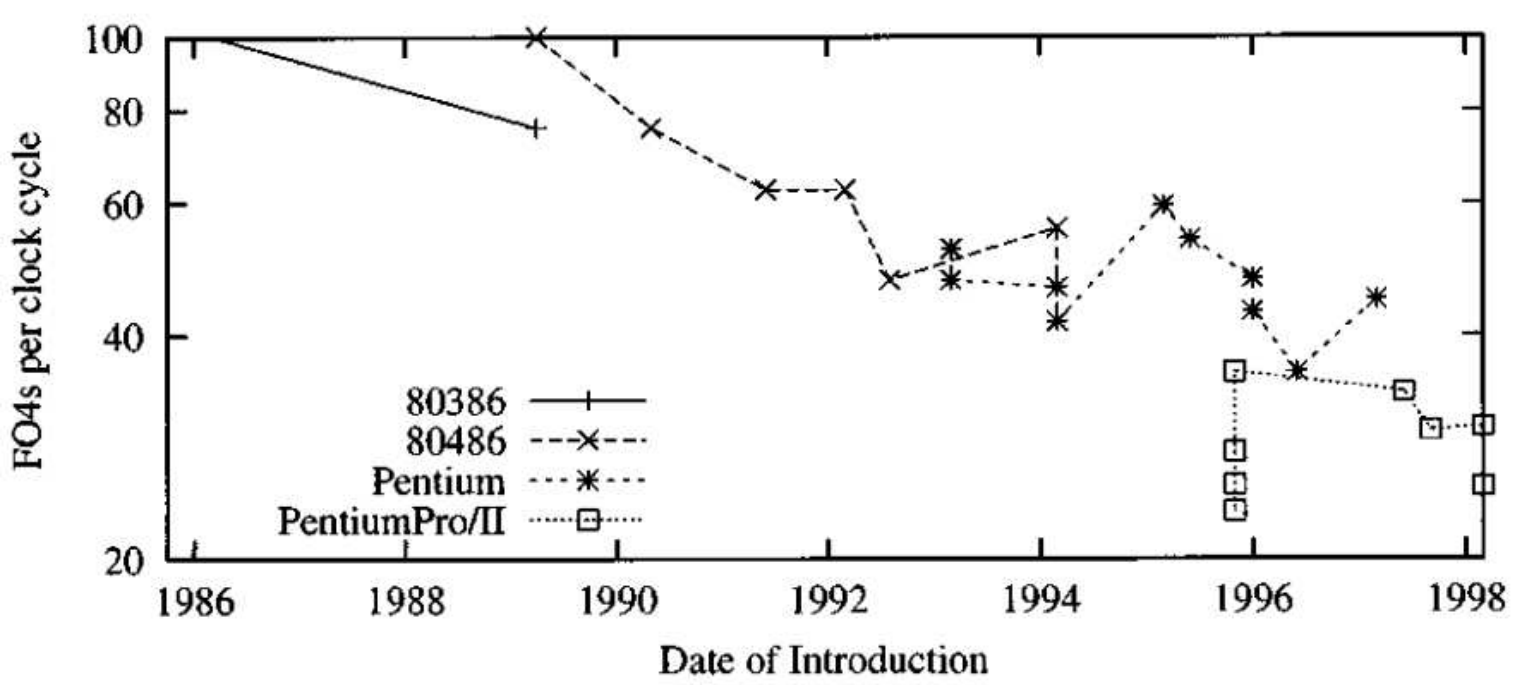

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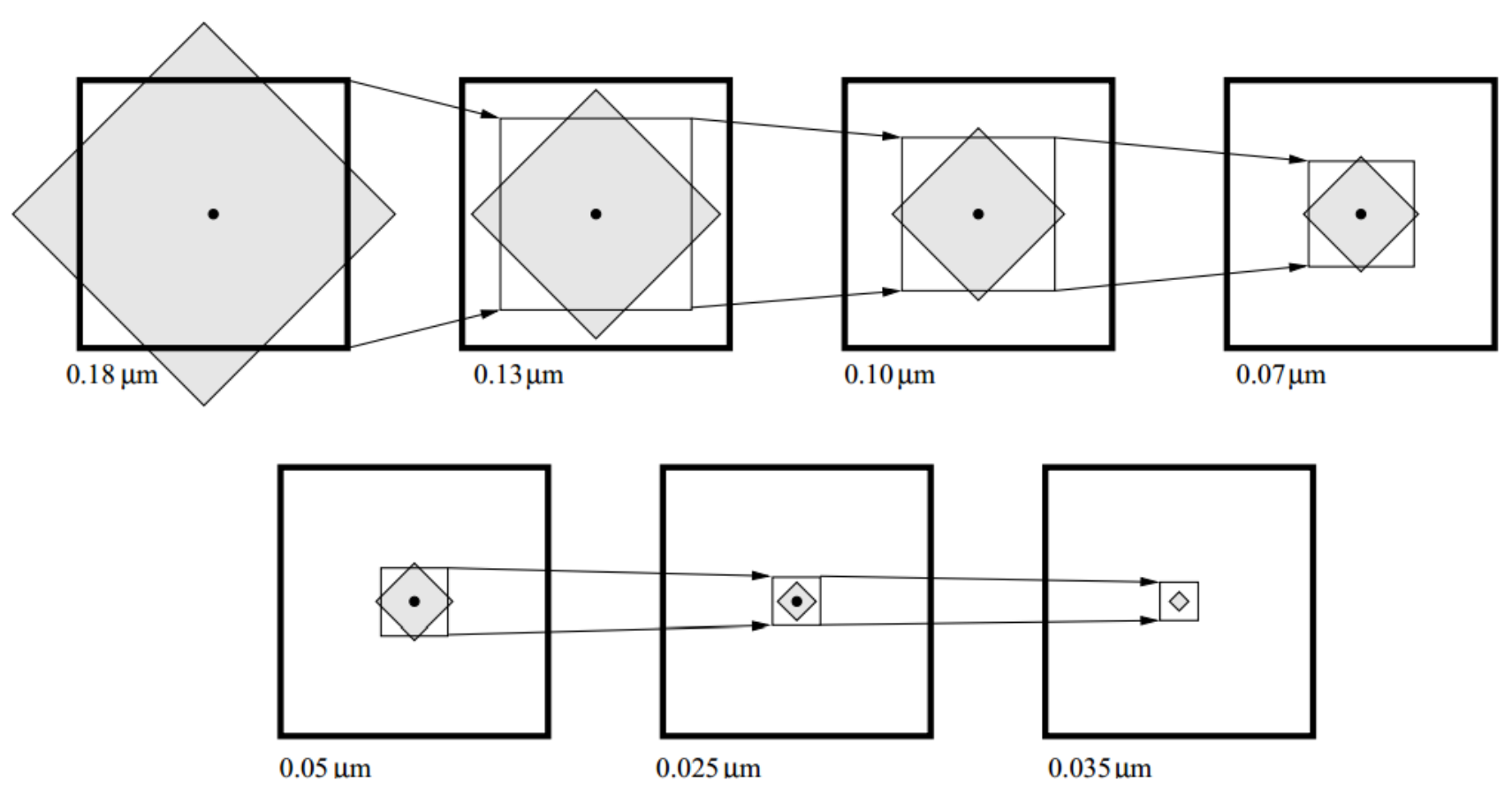

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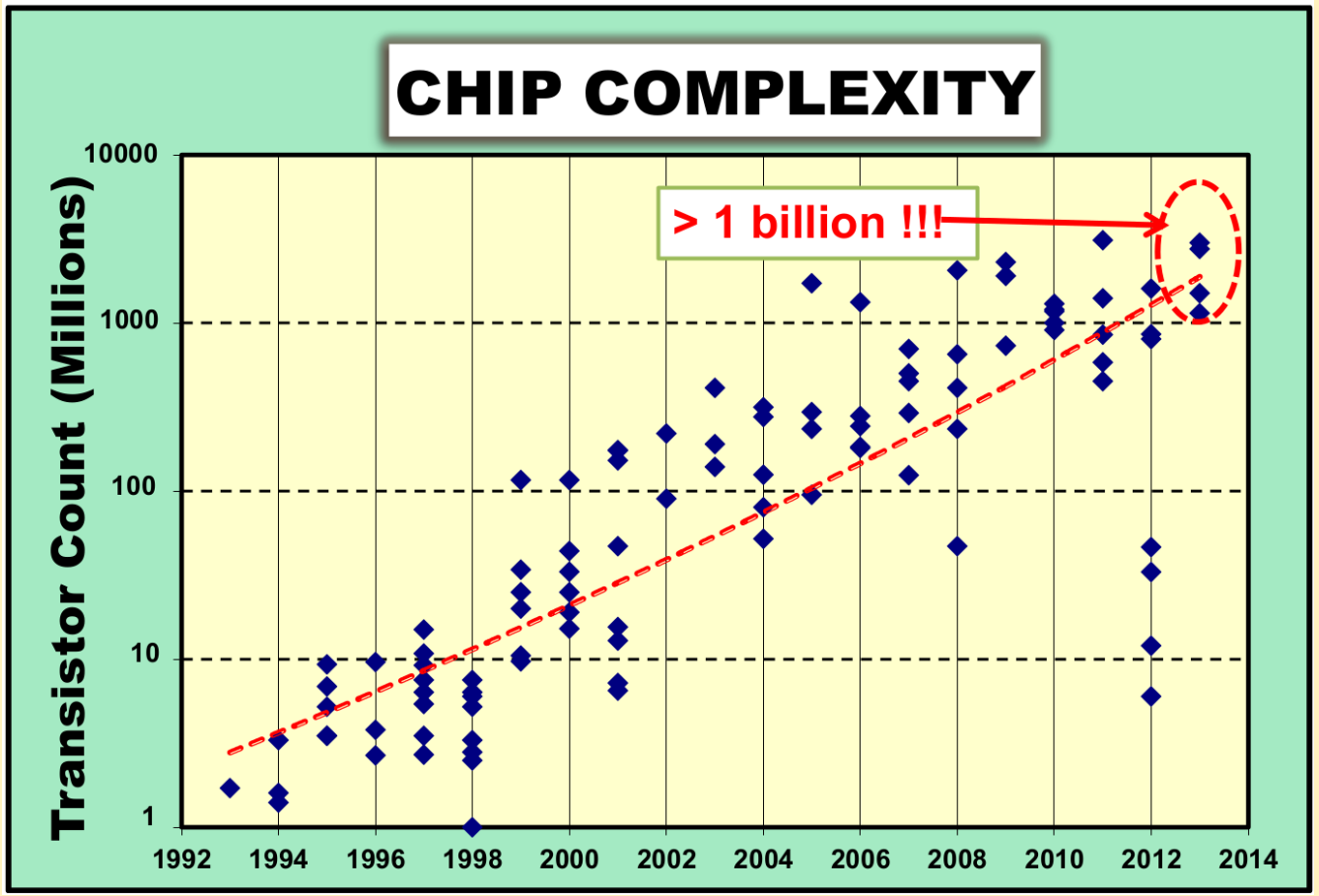
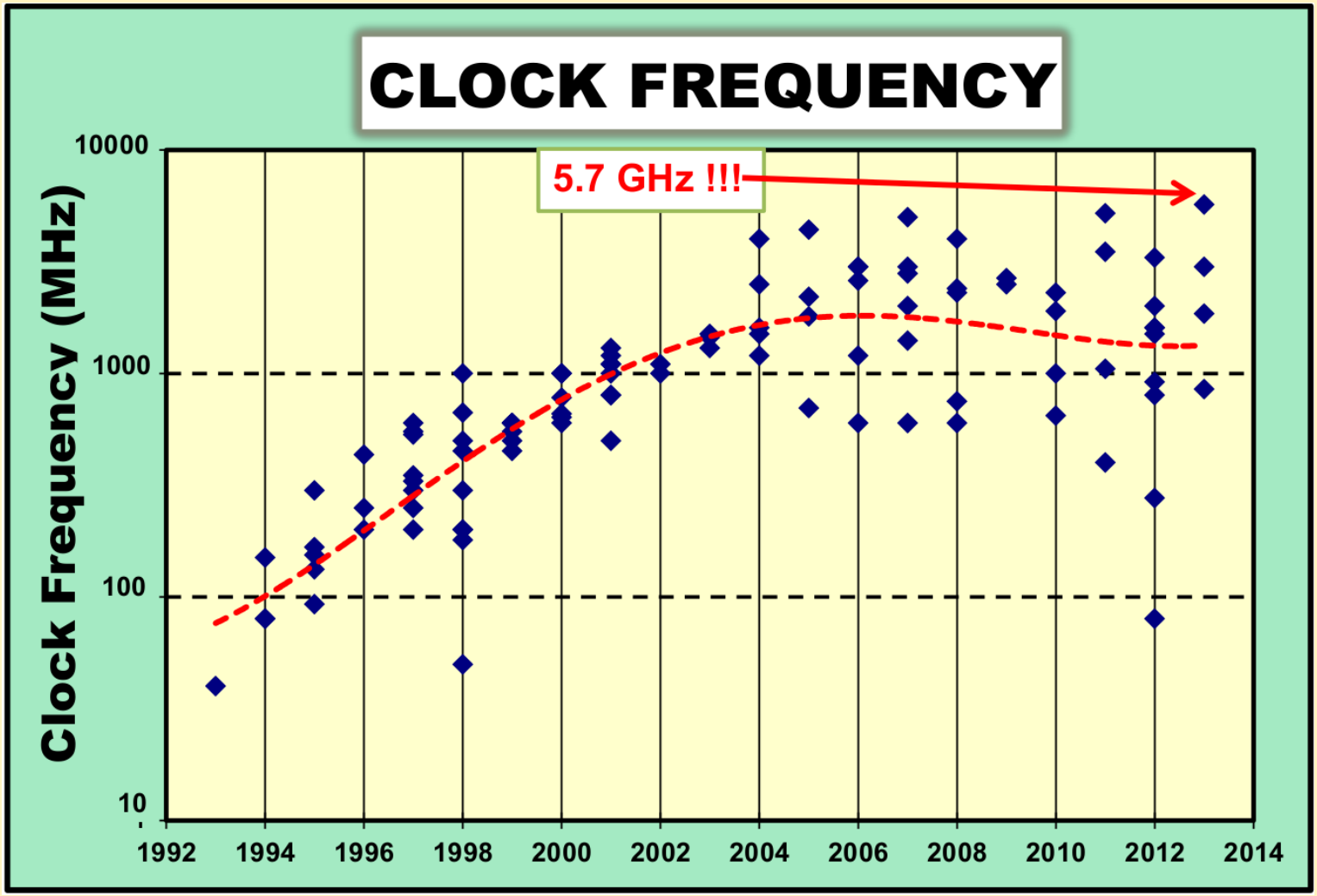
Capacity Trend



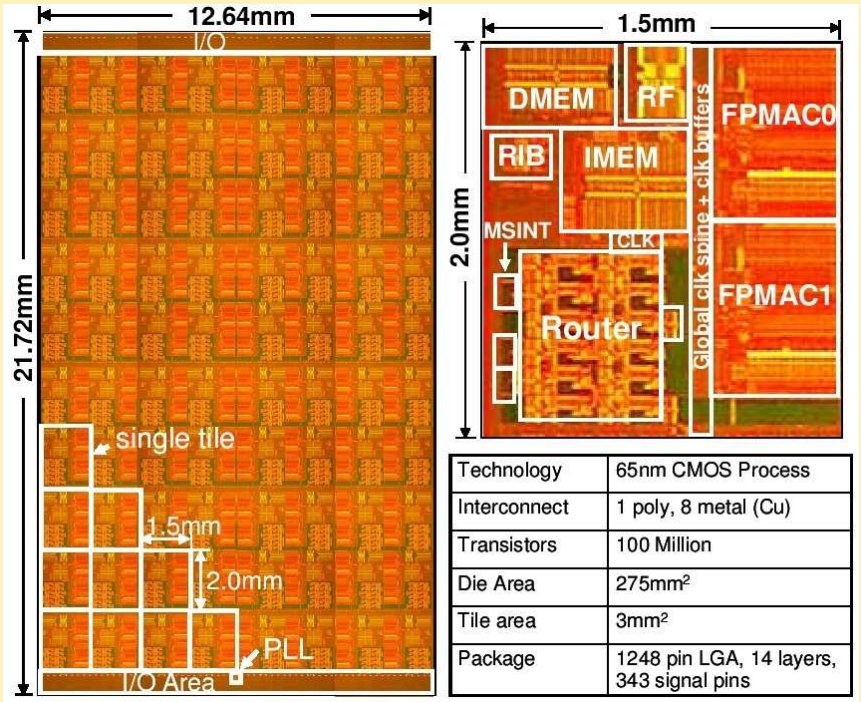
From the ISSCC 2013 Technology Trends

The End of Frequency Scaling



From the ISSCC 2013 Technology Trends

Emergence of NoC



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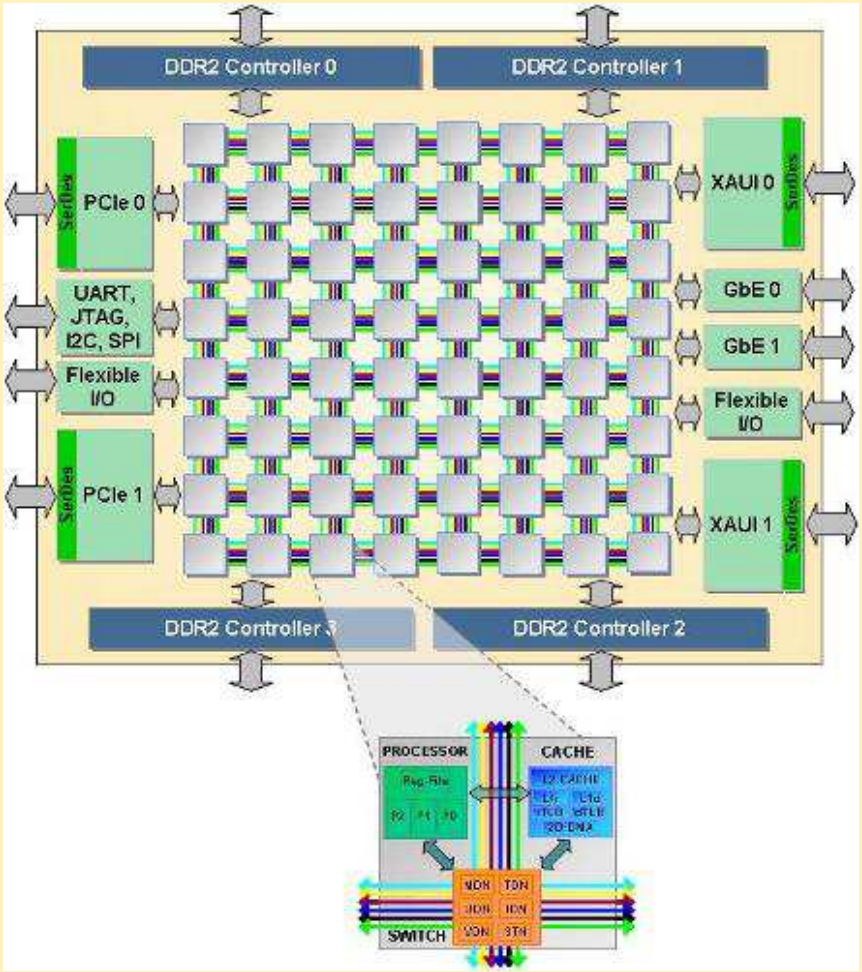
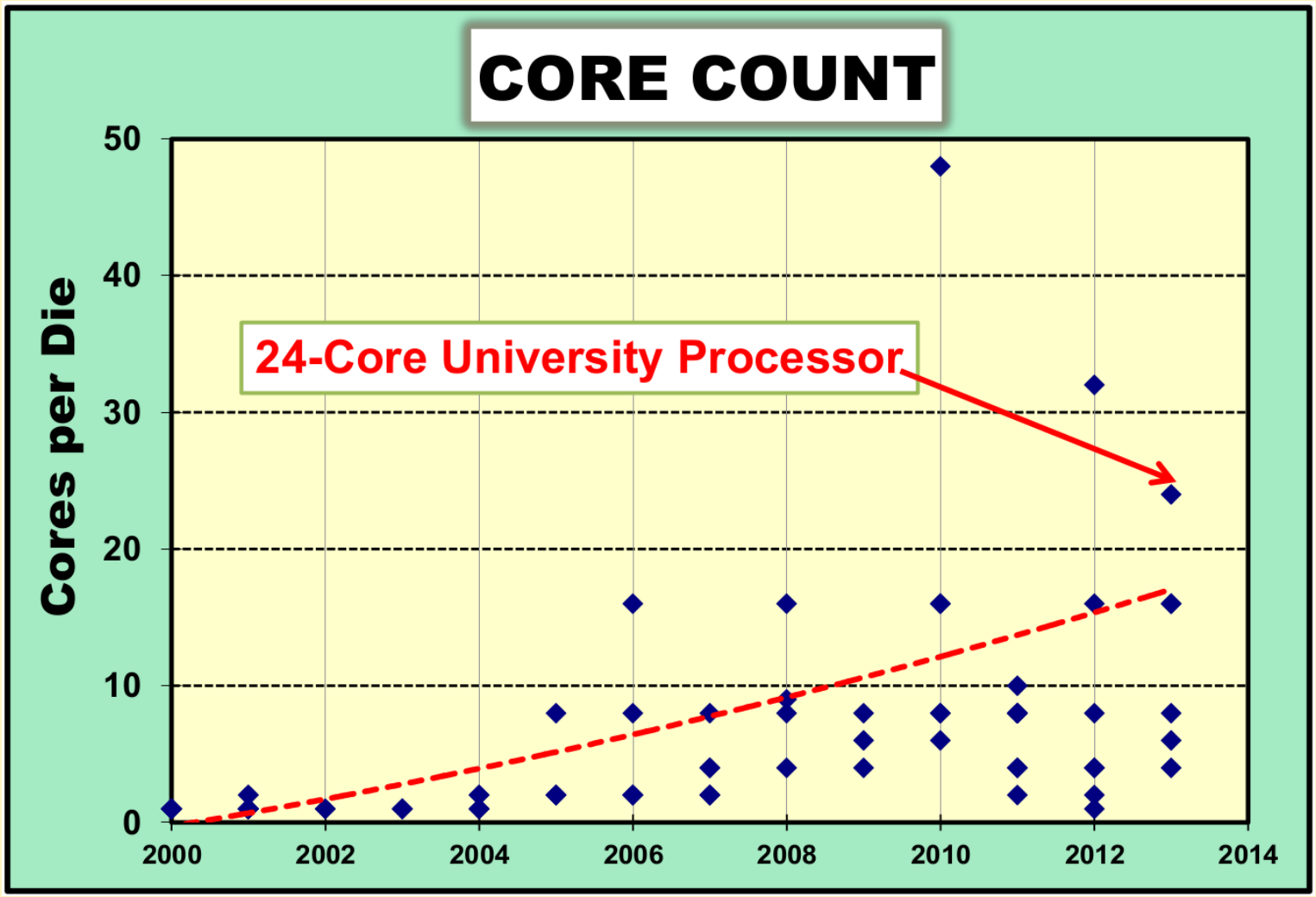
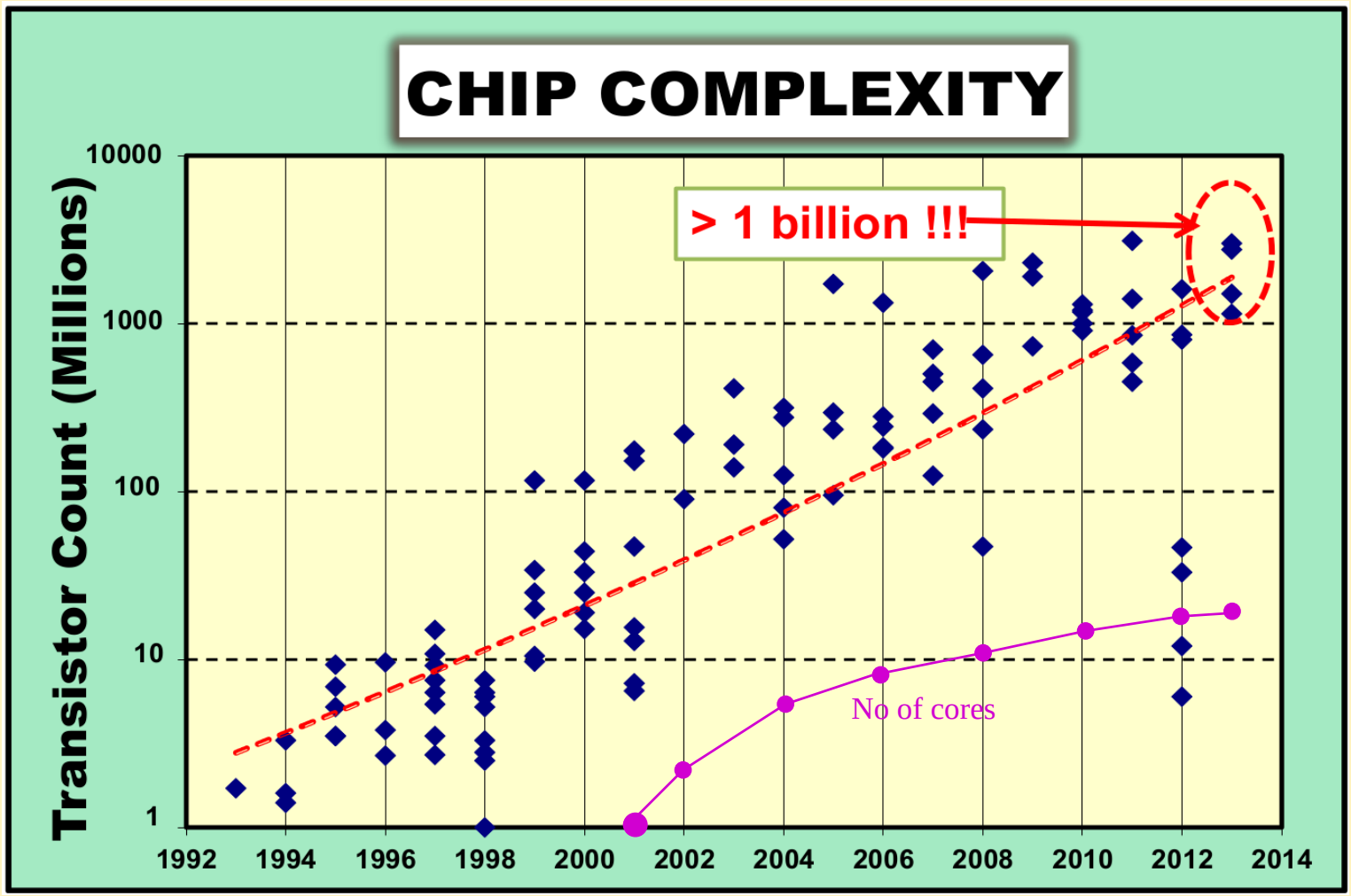


The Multicore Revolution



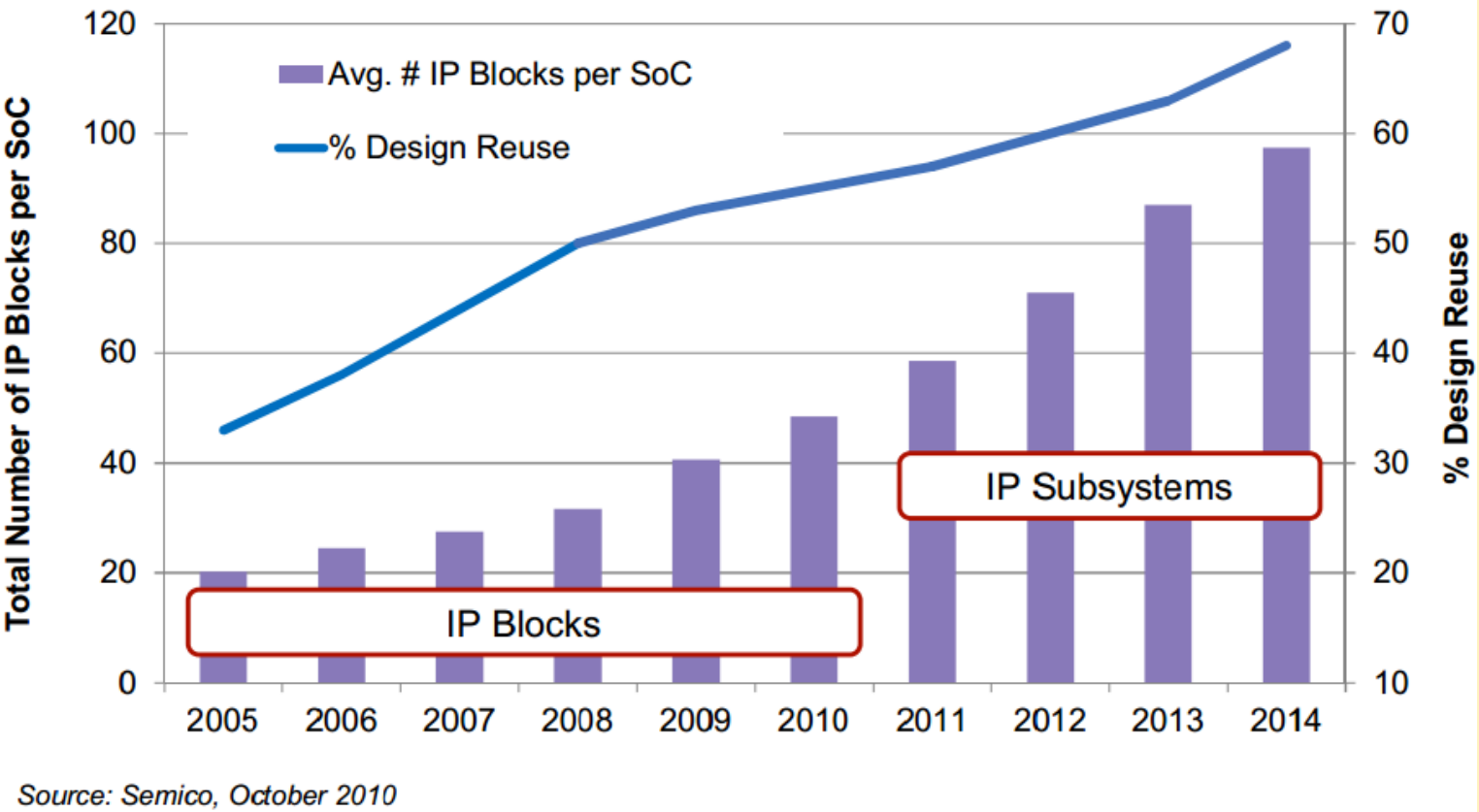
From the ISSCC 2013 Technology Trends

The Multicore Revolution



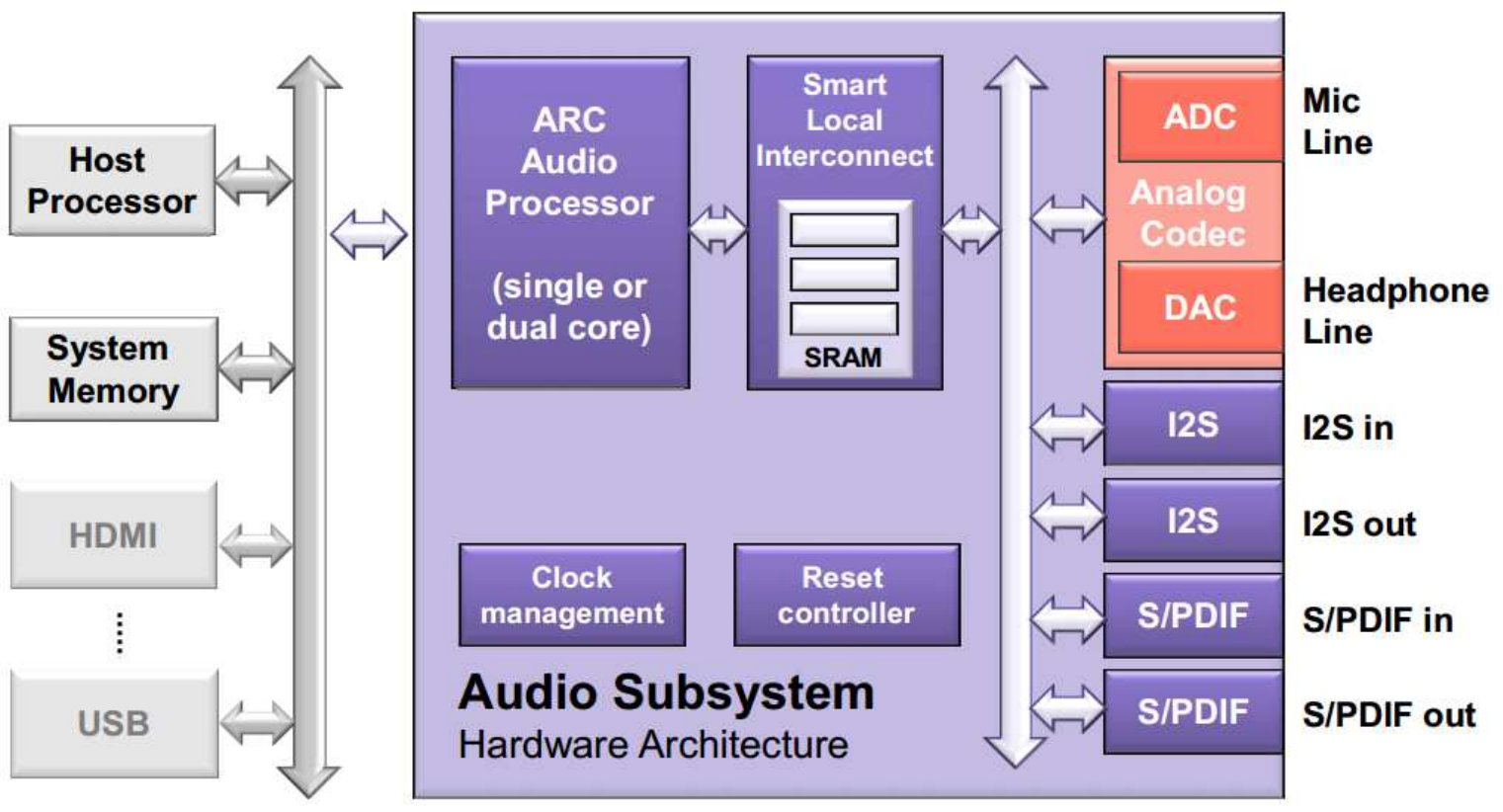
From the ISSCC 2013 Technology Trends

The Reuse of Subsystems



Source: Semico, October 2010

The Reuse of Subsystems



How are Transistors Used?

- More cores and IPs
- SoC infrastructure: interconnect, cache coherence, power management, synchronization, data movement, I/O, test IPs, ...
- Memory, caches, buffers
- IPs become more complex

2013: 3 000 000 000 Transistors

What Next?

2013: 3 000 000 000 Transistors

What Next?

- 22 nm is state of the art
- 14 nm under preparation
- 10 nm is scheduled to go commercial in 2015
- 7 nm is expected in 2020

When Will Moore's Law End?

In 2604

In 2604

Universal Limits on Computation

Lawrence M. Krauss[1] and Glenn D. Starkman[1,2]
[1] *Center for Education and Research in Cosmology and Astrophysics, Department of Physics, and Department of Astronomy, Case Western Reserve University, Cleveland, OH 44106-7079*
[2] *Department of Physics, CERN, Theory Division, 1211 Geneva 23, Switzerland*

The physical limits to computation have been under active scrutiny over the past decade or two, as theoretical investigations of the possible impact of quantum mechanical processes on computing have begun to make contact with realizable experimental configurations. We demonstrate here that the observed acceleration of the Universe can produce a universal limit on the total amount of information that can be stored and processed in the future, putting an ultimate limit on future technology for any civilization, including a time-limit on Moore's Law. The limits we derive are stringent, and include the possibilities that the computing performed is either distributed or local. A careful consideration of the effect of horizons on information processing is necessary for this analysis, which suggests that the total amount of information that can be processed by any observer is significantly less than the Hawking-Bekenstein entropy associated with the existence of an event horizon in an accelerating universe.

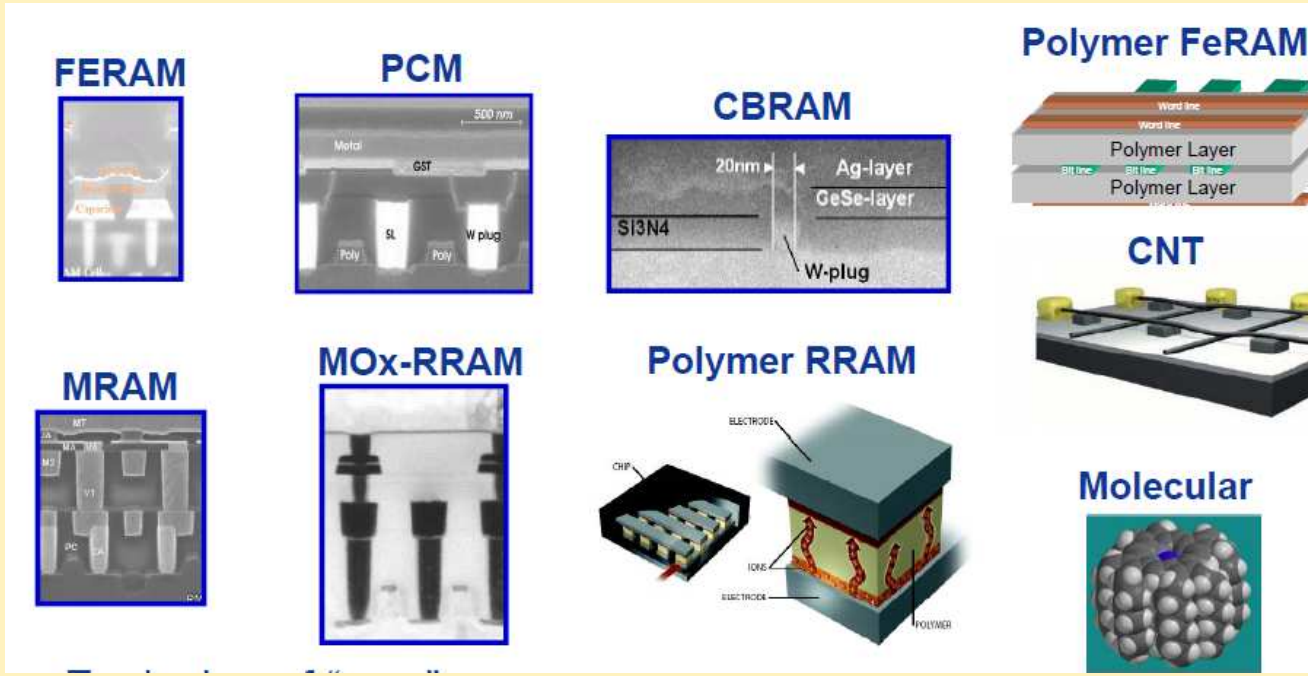
y 2004

Trends

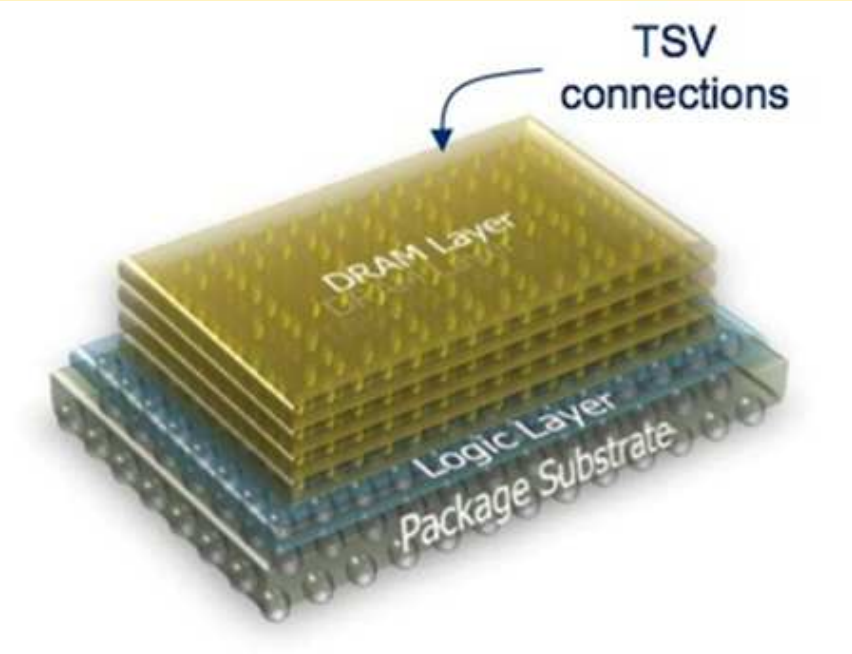
- Many new technologies under development
- Heterogeneity and Specialization
- Integration with the physical world

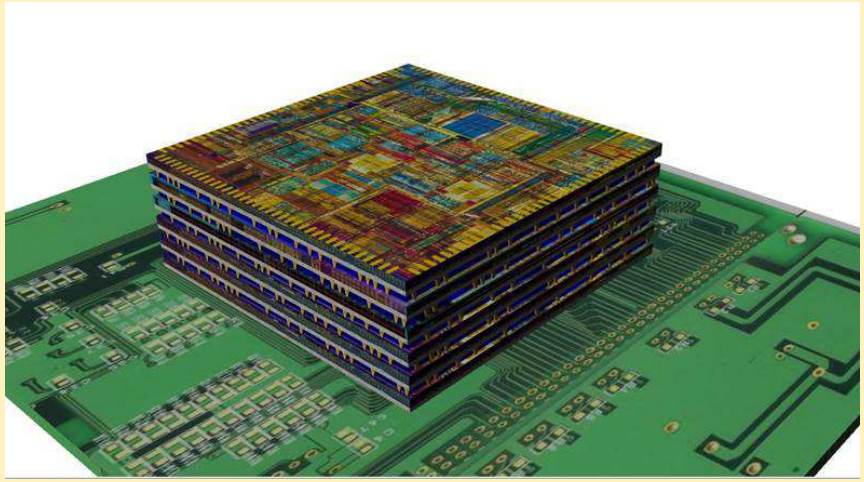
Promising Technologies

- 3D Stacking
- 3D Transistors
- Phase Change RAM
- Spin Torque Transfer RAM
- Memristor
- Hybrid Memory Architectures
- Carbon Nano Tubes
- Organic Electronics
- Functional Materials
- ...

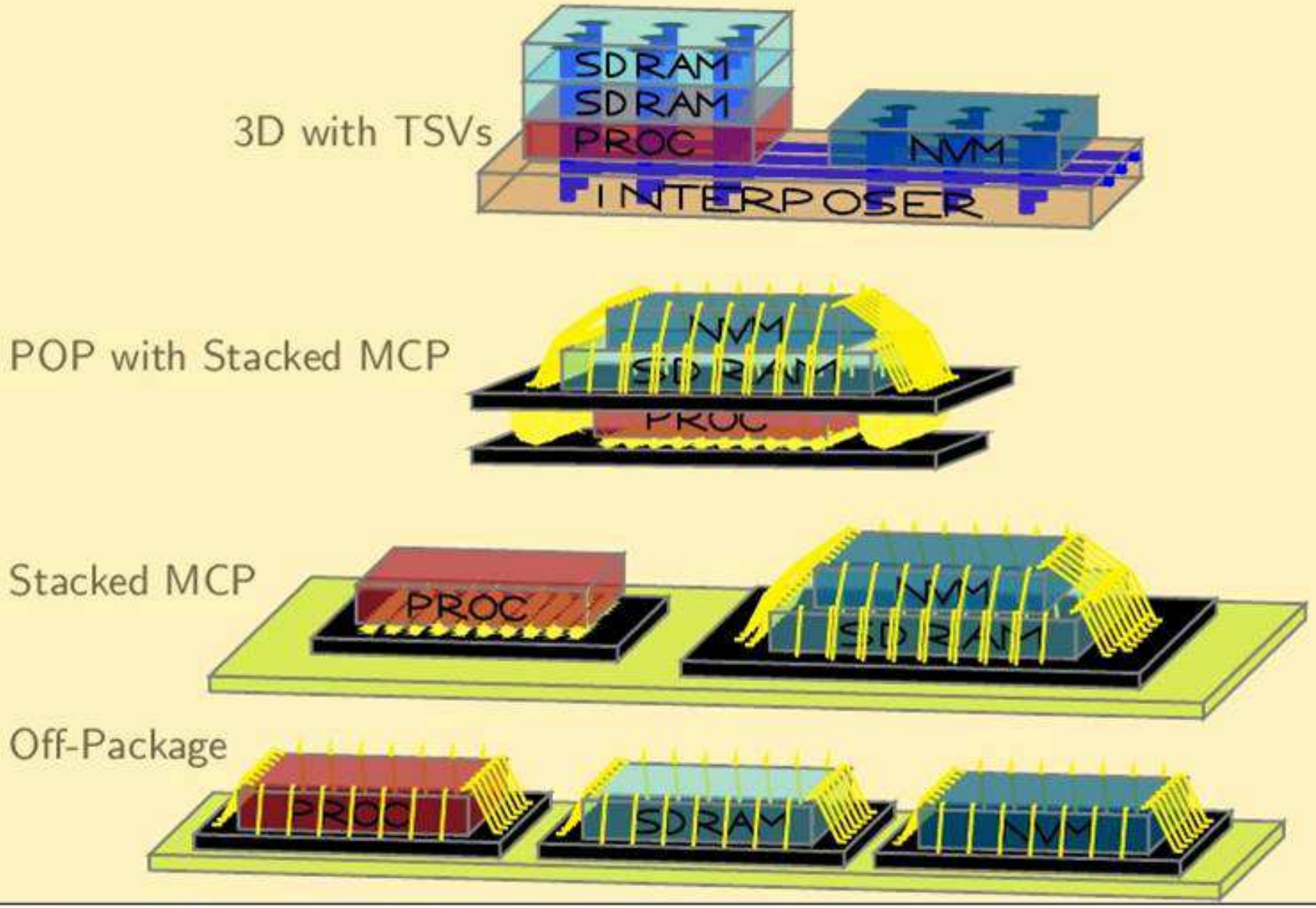


3D Stacking



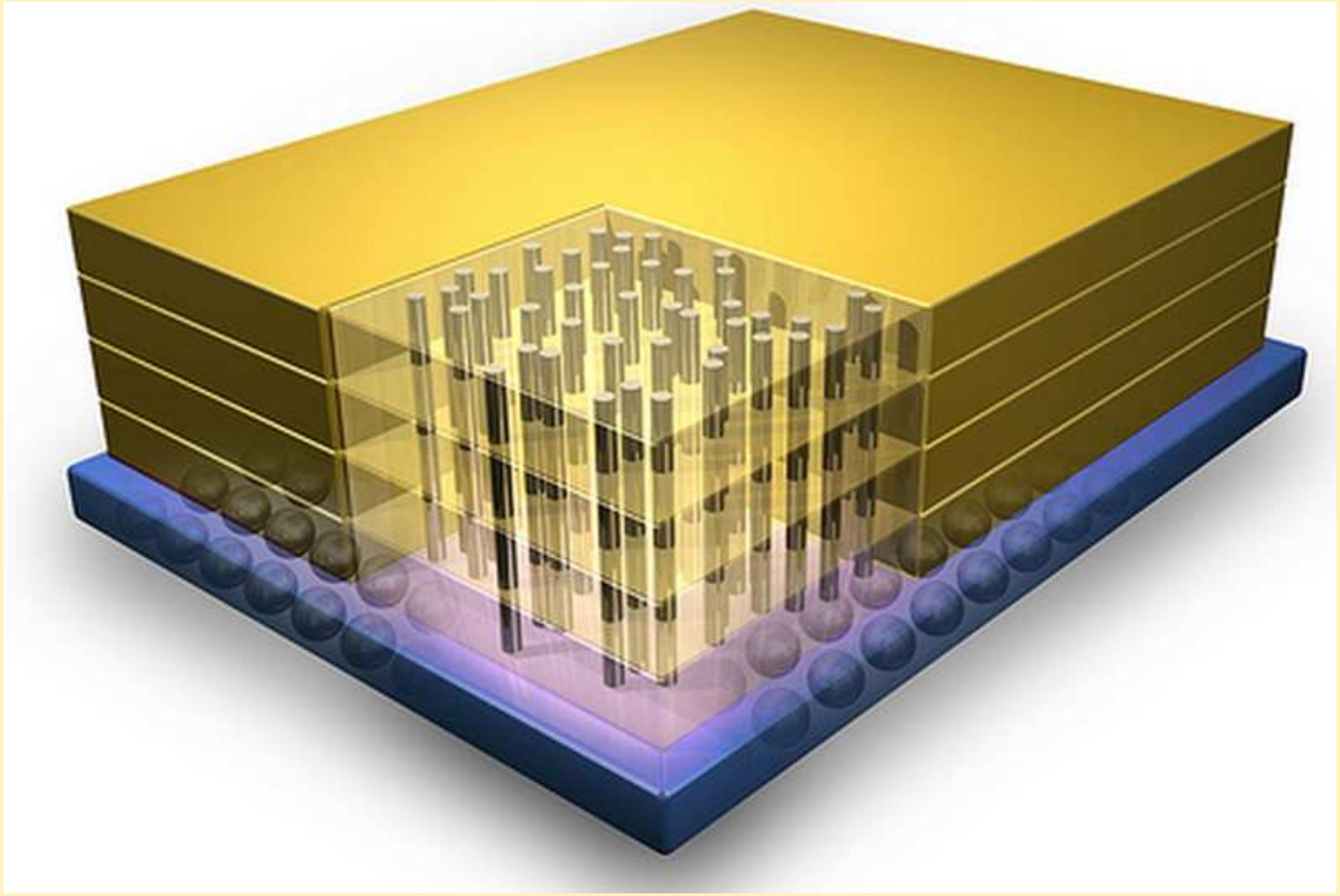


3D Stacking



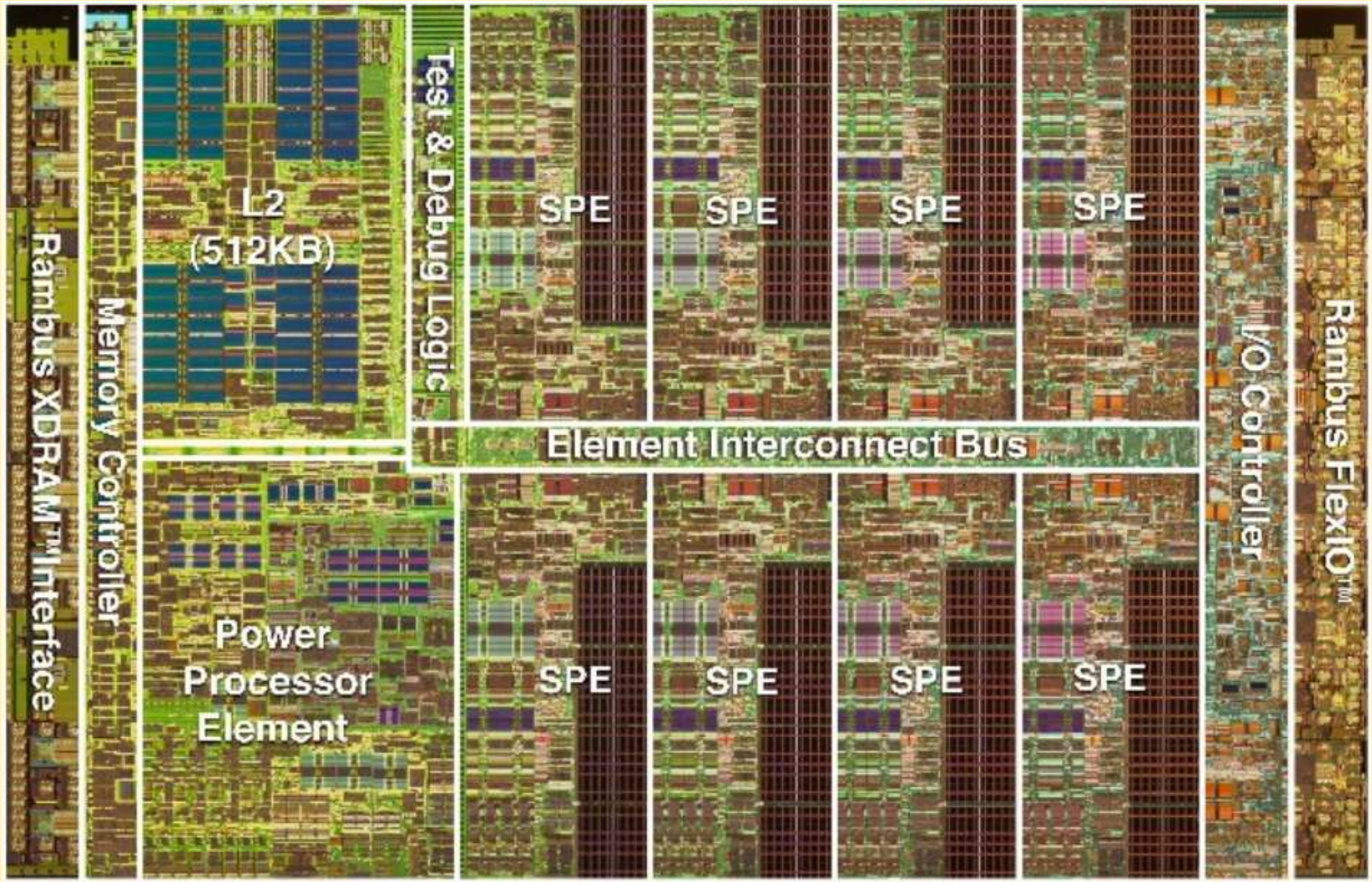
From: Denis Dutois and Ahmed Jerraya. "3D Integration Opportunities for Memory Interconnect in Mobile Computing Architectures". In: *Future Fab International* 34 (July 2010)

3D Stacking



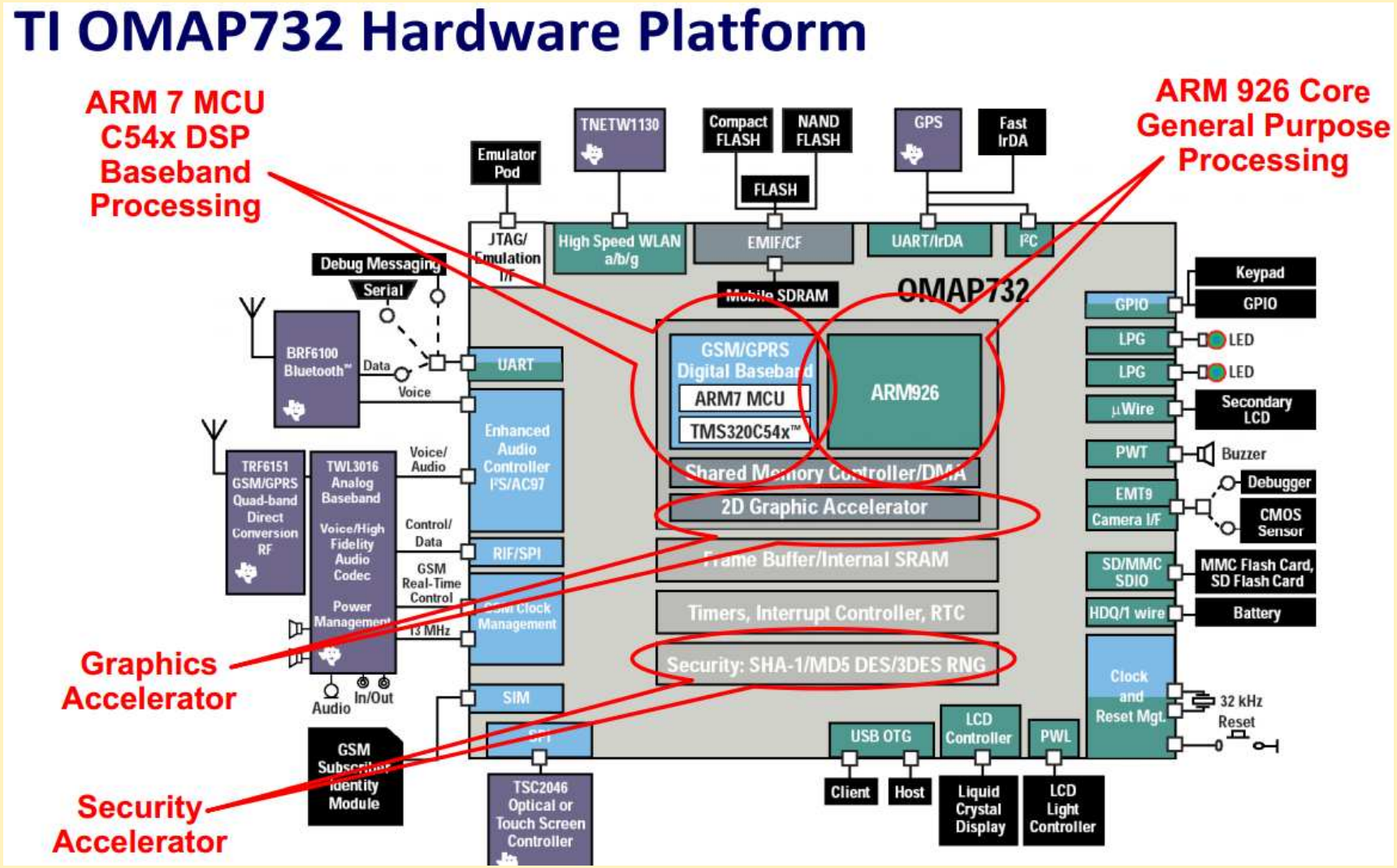
Micron 2014: 4 GB package, 4 dies stacked in a $31 \times 31\text{mm}^2$ package

The Era of Heterogeneity



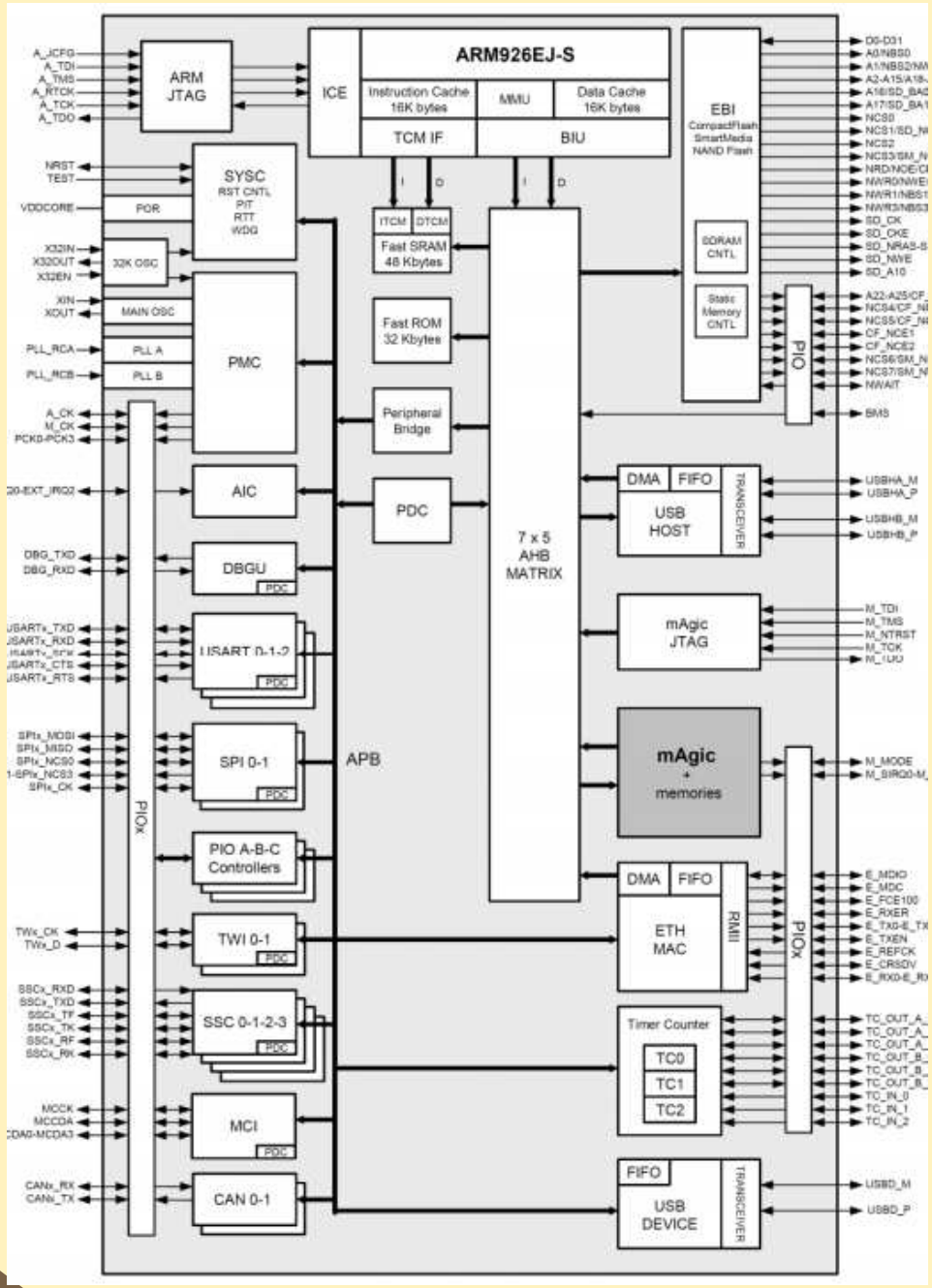
IBM Cell Processor

The Era of Heterogeneity



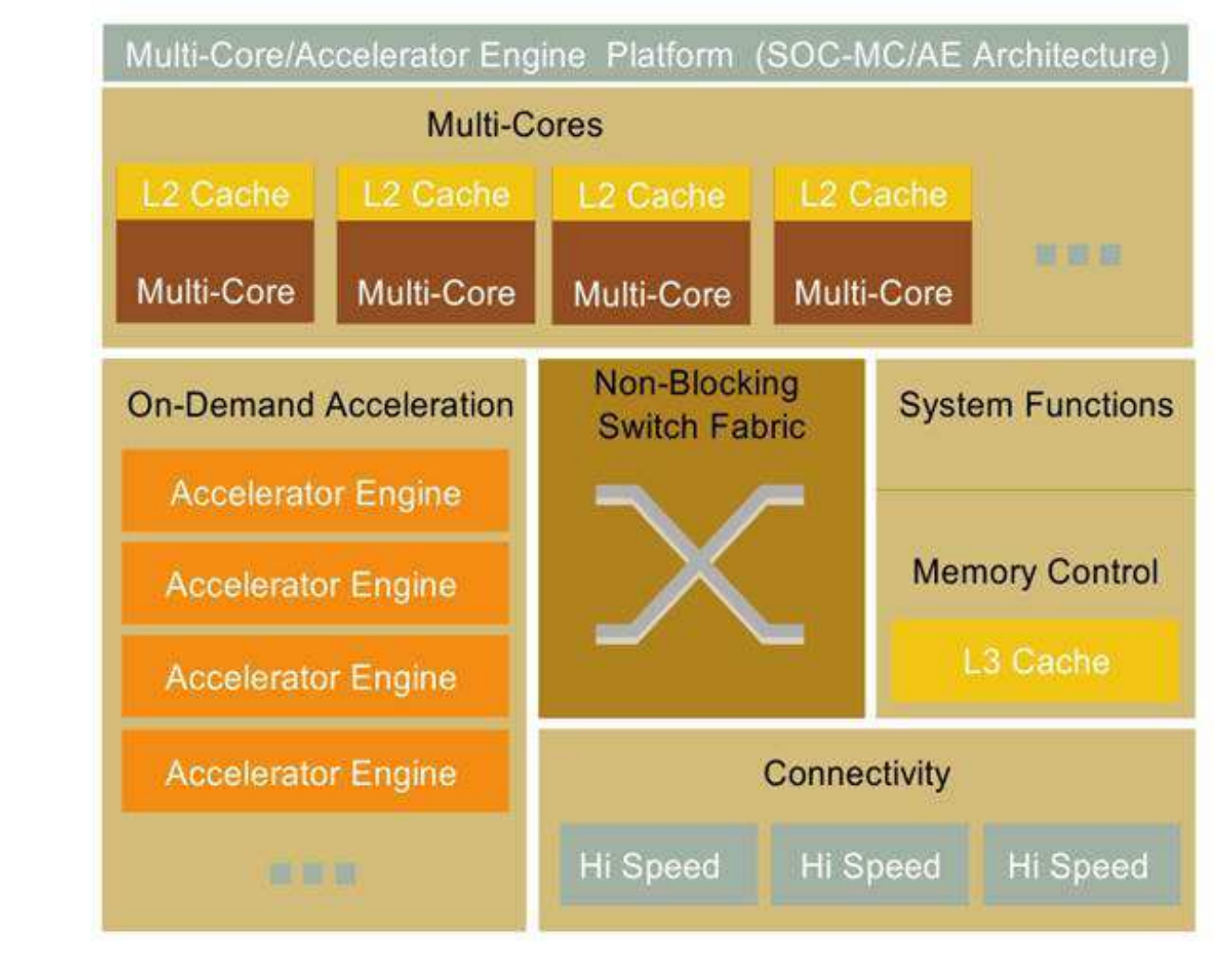
TI OMAP Platform

The Era of Heterogeneity



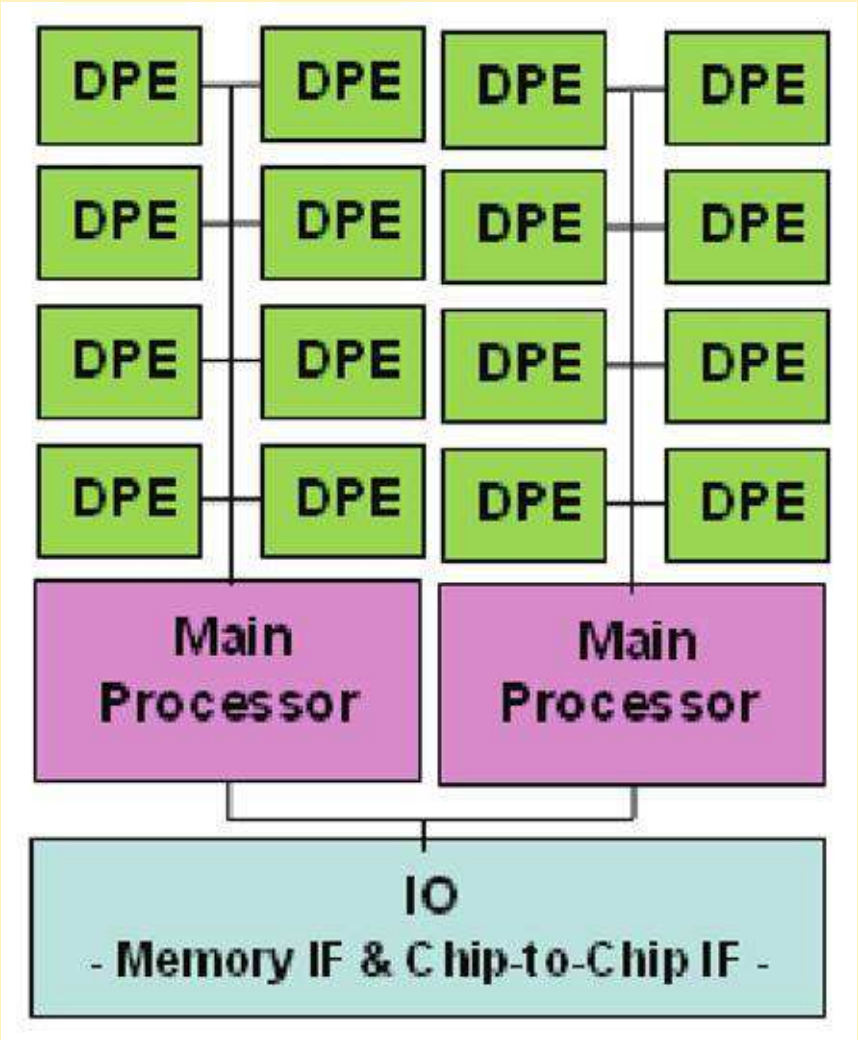
DIOPSIS 940 for audio, speech processing, automotive sound, robotics

The Era of Heterogeneity



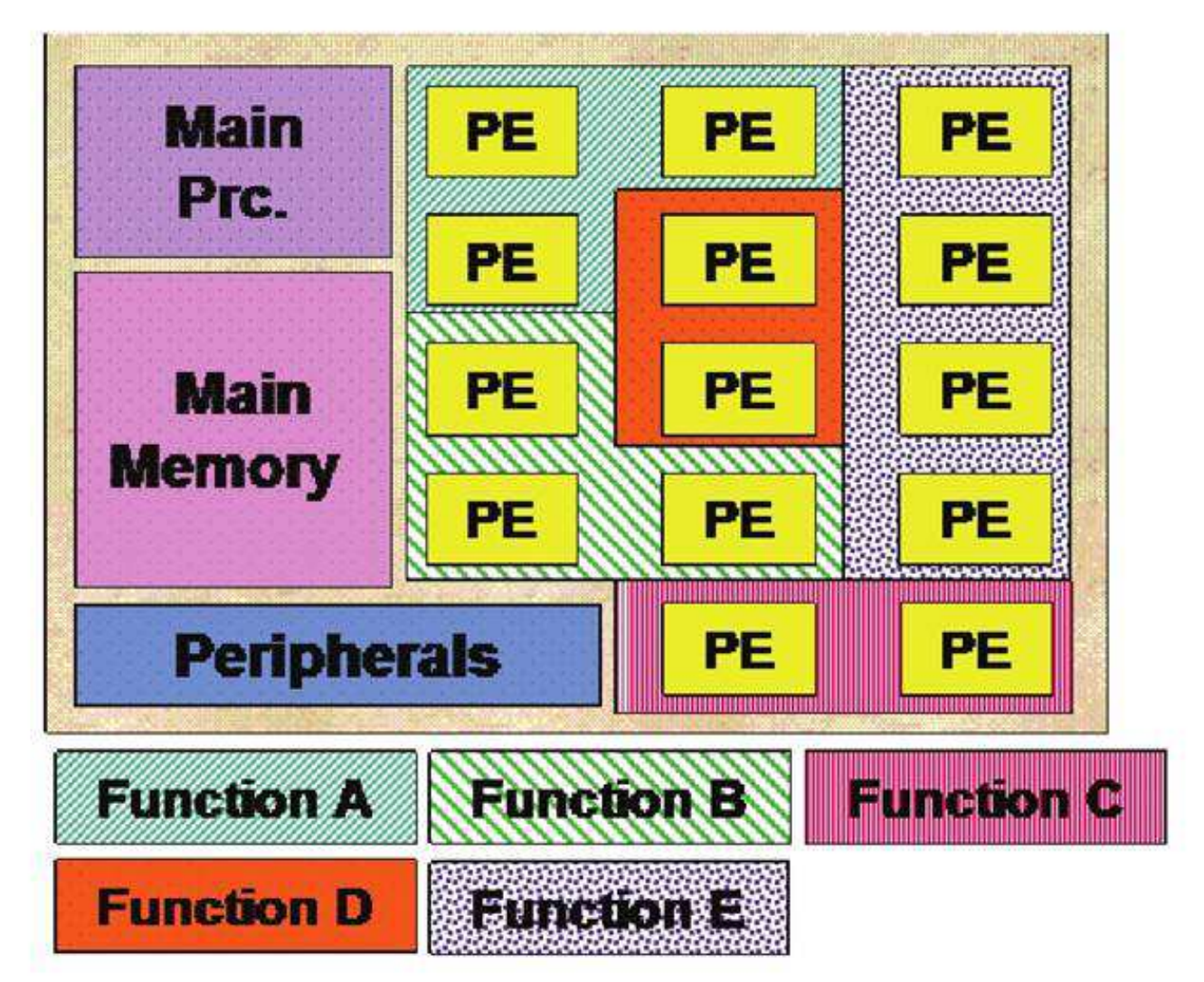
SoC Networking Architecture (ITRS)

The Era of Heterogeneity



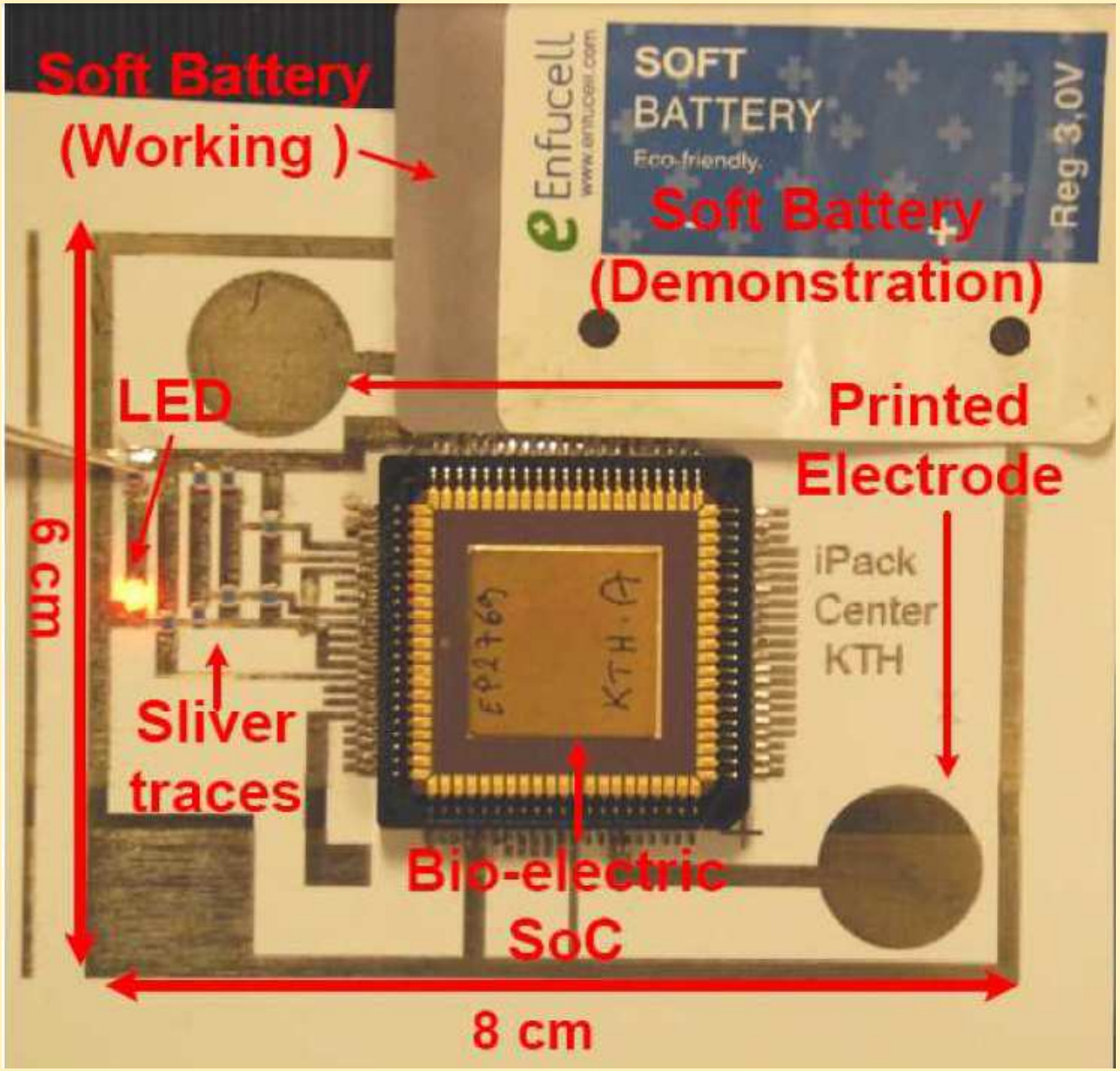
SoC Consumer Stationary (ITRS)

The Era of Heterogeneity



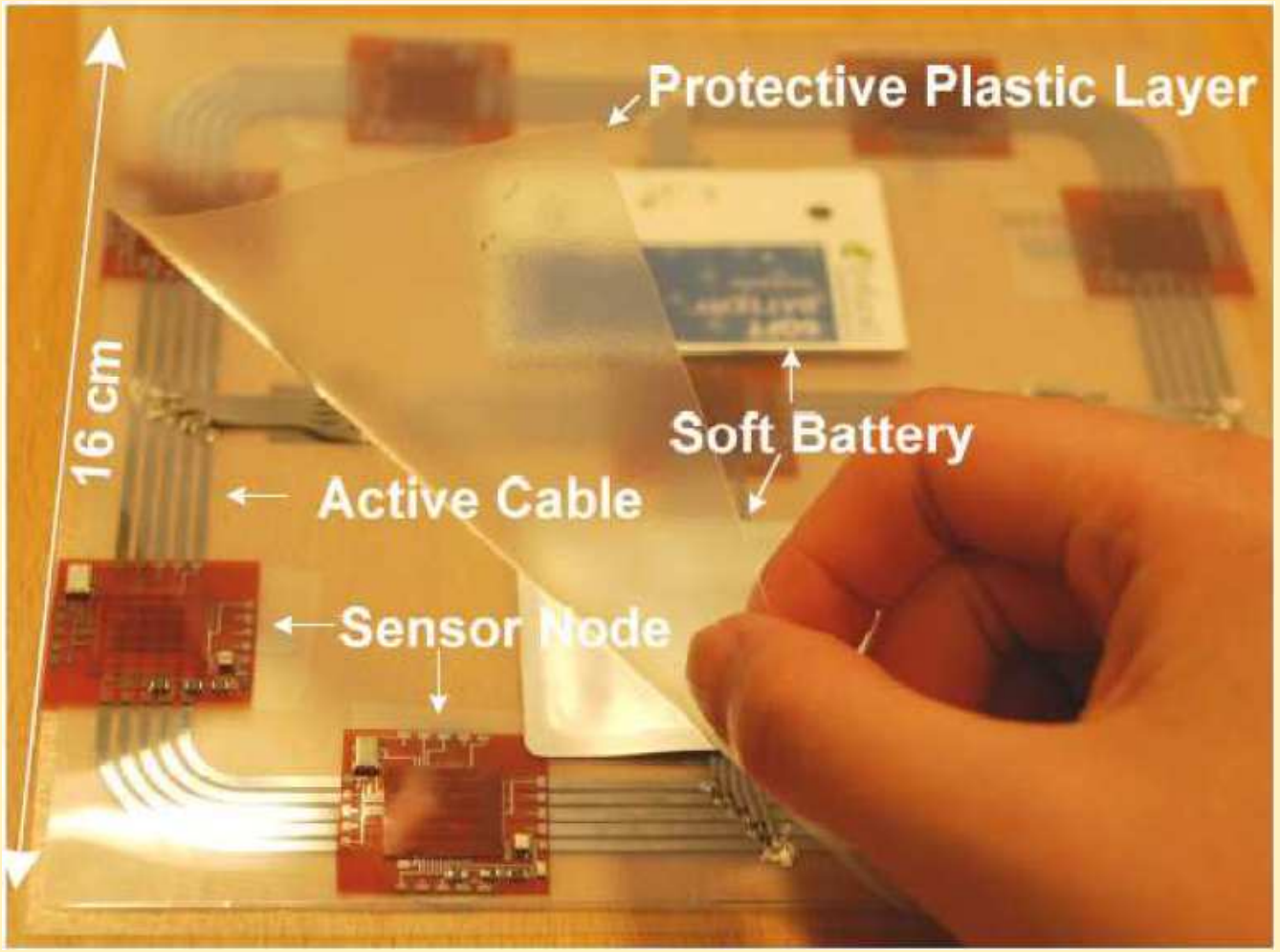
SoC Consumer Portable (ITRS)

Heterogeneous Integration



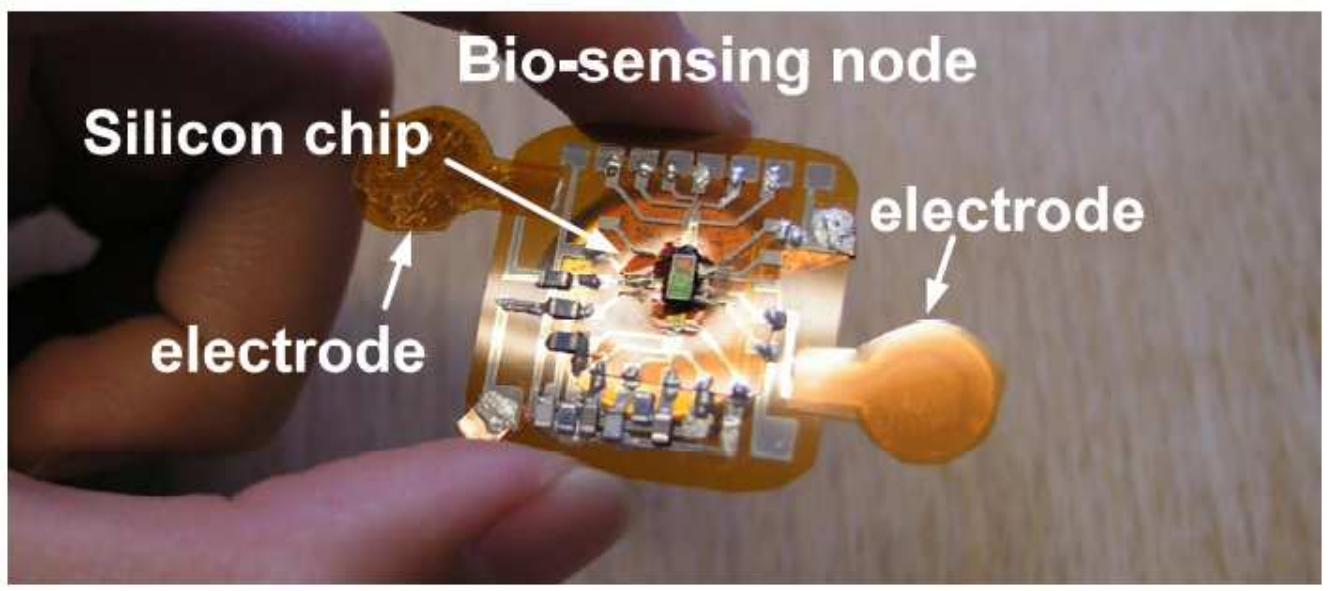
rtesy of KTH

Heterogeneous Integration



Courtesy of KTH

Heterogeneous Integration



Courtesy of KTH

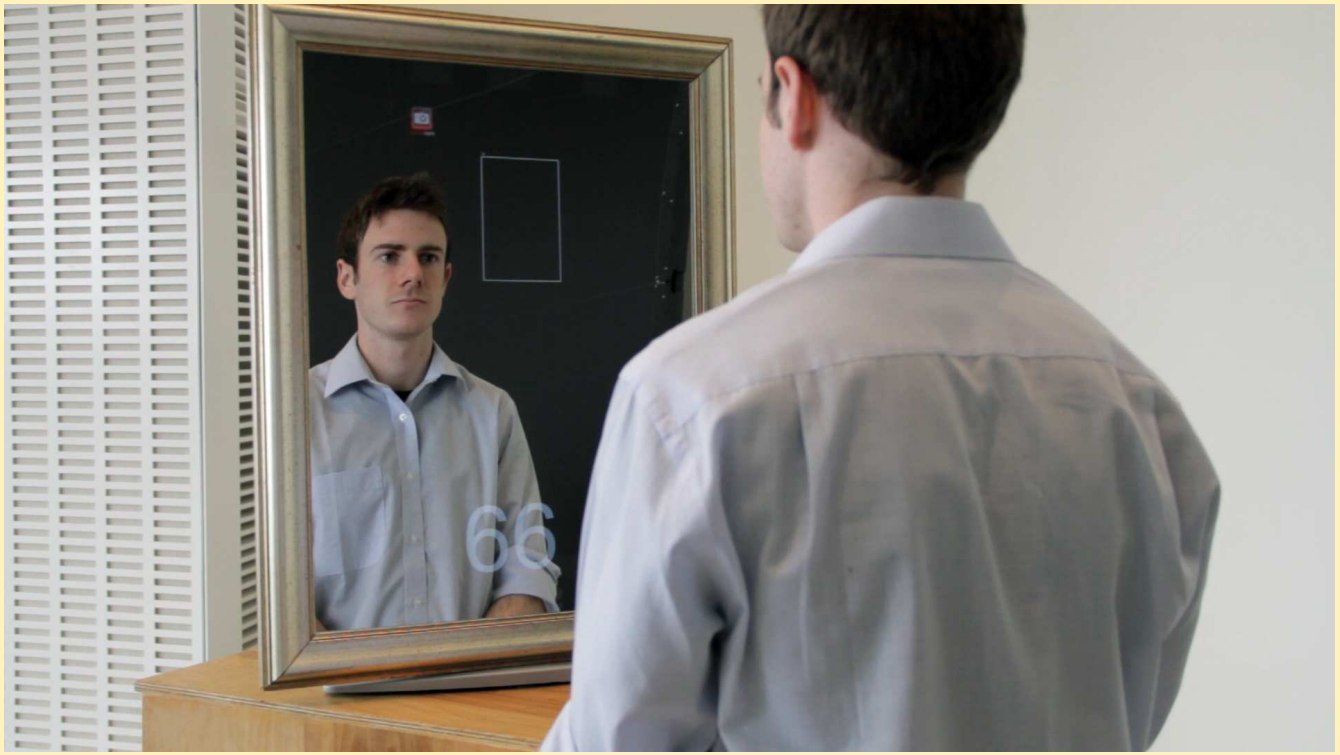
Lighting Control

Courtesy of MIT Media Lab

Eyesight Test

Courtesy of MIT Media Lab

Non-Invasive Monitoring



Courtesy of MIT Media Lab

The World in 2025

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The World in 2025

- Moore's Law has faded away
- General purpose computing has become a niche market
- We have a wealth of materials and technologies at hand
- New value comes from
  1. **Devising new solutions to interesting problems**
  2. Novel, heterogeneous integration
  3. New sensors and actuators
  4. New materials including bio-processes
  5. Further IC integration