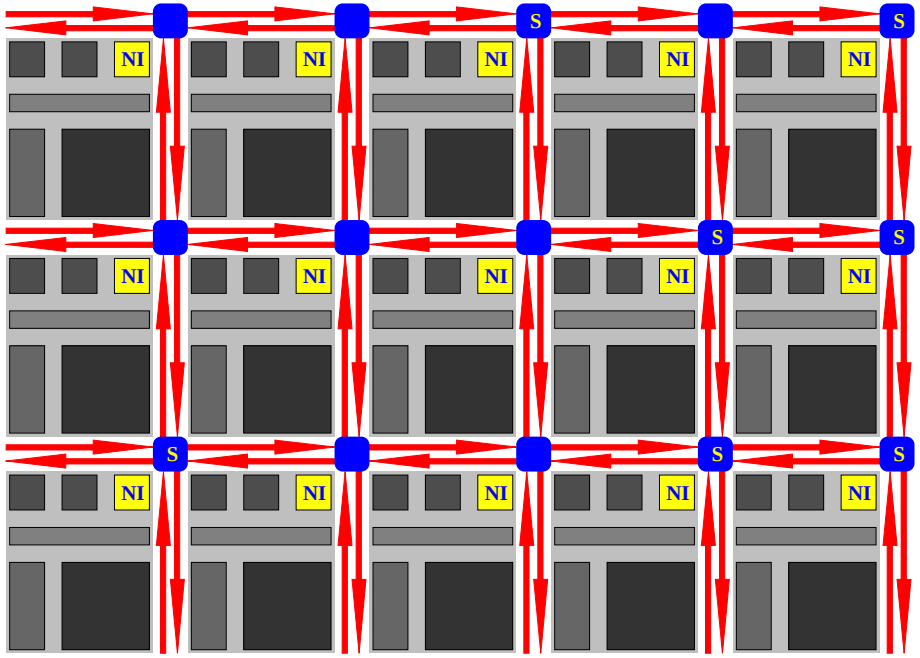
Network on Chip



Axel Jantsch, Zhonghai Lu, Shashi Kumar, Ahmed Hemani, Mikael Millberg, Rikard Thid, Johnny Öberg, Erland Nilsson, Xiaowen Chen, Yuang Zhang, Abdul Naeem, Sandro Penolazzi, Jean-Michel Chabloz, Shaoteng Liu, Chaochao Feng, Wenmin Hu, et al.

Royal Institute of Technology, Stockholm

December 2010

VETENSKAP OCH KONST

Overview

KTH Research on NoC

Topology and Structure

Routing

Switching

Flow Control

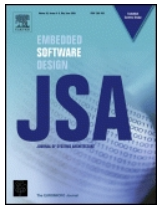
NoC Research at KTH

- November 2000: First papers with NoC in the title

  Ahmed Hemani, Axel Jantsch, Shashi Kumar, Adam Postula, Johnny Öberg, Mikael Millberg, and Dan Lindqvist. *Network on chip: An architecture for billion transistor era*. In Proceeding of the IEEE NorChip Conference, November 2000.

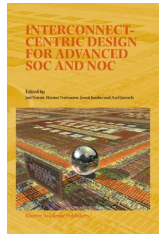
- September 2001: First half-day Workshop on NoC at European Solid State Circuits Conference ESSCIRC
- 2003: First NoC book February 2003: *Networks on Chip*, Kluwer

- February 2004: First Special issue on NoC in the Journal of System Architecture (JSA)



NoC Research at KTH

- April 2004: Second NoC book: *Inteconnect Centric Design for Advanced SoCs and NoCs*, ed.: Jari Nurmi, Hannu Tenhunen, Jouni Isoaho, and Axel Jantsch



- 2007: Book *Networks on Chip* translated to Chinese

- 2011: *3D Integration for NoC Based SoC Architectures*, Editors: Abbas Sheibanyrad, Frédéric Pétrot, Axel Jantsch
- 2011: *Scalable Multi-core Architectures: Design Methodologies and Tools*, Editors: Axel Jantsch and Dimitrios Soudris
- In summary:
  - ⋆ Top citation count in Google Scholar under term "Network on Chip"
  - ⋆ > 40 keynotes, invited talks, tutorials on NoC
  - ⋆ > 100 publications on NoC
  - ⋆ One of the pioneers and most productive groups on this topic

NoC Keynotes, Invited Talks and Tutorials

- *Networks on chip*. Presentation at the Conference RadioVetenskap och Kommunikation, June 2002.
- *Network on chip architecture*. Presentation at the EXCITE Workshop, Helsinki, November 2002.
- *Networks on chip: A paradigm change?* Presentation at the SOCWare Day, Kista, November 2002.
- *NoCs: A new contract between hardware and software*. Keynote at the Euromicro Symposium on Digital System Design, September 2003.
- *The Nostrum network on chip*. Invited presentation at ProRISC, November 2003.
- *The nostrum network on chip*. Invited seminar at Linkping University
- *The nostrum network on chip*. Invited Seminar at bo Akademi, Turku, Finland, March 2005.
- *NoC: A new contract between hardware and software?* Invited seminar at Lancaster University, October 2005.

NoC Keynotes, Invited Talks and Tutorials

- *The Nostrum network on chip*. Invited presentation at the International Symposium on System-on-Chip, Tampere, Finland, November 2005.
- *Standards for NoC: What can we gain?* Invited presentation at the Workshop on Future Interconnect and NoC, DATE, March 2006.
- Tiberius Seceleanu, Axel Jantsch, and Hannu Tenhunen. *On-chip distributed architectures*. Tutorial at the International SoC Conference, September 2006. Austin, Texas.
- *Communication performance in network-on-chips*. Short course at Tallinn Technical University, October 2006.
- *Models of computation for networks on chip*. Invited talk at the Sixth International Conference on Application of Concurrency to System Design, June 2006.
- *Network layer communication performance in networks on chip*. Tutorial at the Asian Pacitific Design Automation Conference, January 2008.

NoC Keynotes, Invited Talks and Tutorials

- *Quality of service in networks on chip*. Invited Seminar at the Research Center Telecommunciation Vienna (FTW), April 2008.
- *Resource allocation for quality of service on-chip communication*. Invited seminar at the University of Cantabria, Santander, Spain, February 2009.
- *Performance analysis and dimensioning of bandwidth and buffer capacity*. Section I of Full Day Tutorial Tutorial on Networks on Chip at the NoC Symposium 2007, May 2007.
- *NoC: State of the art, trends and challenges*. Section I of Full Day Tutorial NoC at the Age of Six: Advanced Topics, Current Challenges and Trends at DATE 2007, April 2007.

NoC Community Service

- Special issue on NoC in the Journal of System Architecture (JSA) in 2004
- OCP NOC Benchmarking Working Group, one of the initiators and main contributors, from 2006
- Steering Group of NoC Symposium since 2007
- TPC member for NoCS 2007-2009
- Co-organizer of Workshop on Diagnostic Services in Networks on Chip, 2007 (DATE), 2008 (DAC), 2009 (DATE)
- TPC co-chair for NoCS 2009
- DATE NOC Topic chair 2008, 2009
- TPC member for NoCARC 2008, 2009
- Special section in TCAD on NoC in 2010
- NOC book planned for 2010 based on EU FP7 MOSART project

NoC Projects

- NOCARC: Network-on-Chip Architecture, 2001-2004, Vinnova, Partners: Ericsson, Nokia, VTT
- NoC Design Methodology, 2001-2004, SSF
- NoC Evaluation, 2002-2005, SSF
- SPRINT, 2005-2008, EU FP6
- MOSART 2008-2010, EU FP7
- ELITE 2008-2010, EU FP7
- NoC Performance Evaluation, 2009-2011, VR

SPRINT
Open SoC Design Platform for Reuse and Integration of IPs

- EU FP6, 2005-2008
- QoS Communication, protocols and interfaces
- Partners: NXP, ARM, ST
- Main Result:
  - ⋆ Flow regulation based on Network Calculus
  - ⋆ Flow identification for QoS provision
  - ⋆ Device Level Interface (DLI) specification for QoS support
  - ⋆ ARM extends AMBA AXI protocol for QoS support based on SPRINT results

MOSART

Mapping Optimization of Multi-core Architectures

- EU FP7, 2008-2010
- Memory and Data Management for MultiCore NoCs (McNoC)
- Power management and clocking
- Partners: Thales, CoWare, IMEC, VTT, ICCS, Arteris
- Main Results so far:
  - ⋆ Date Management Engine, Patent submitted
    - ∗ Distributed Shared Memory support
    - ∗ Cache coherence
    - ∗ Memory consistency
    - ∗ Dynamic memory allocation and ADT support
  - ⋆ Hierarchical power management archtiecture
  - ⋆ Globally Ratio-synchronous Locally Synchronous clocking scheme (GRLS)

ELITE
Extended Large (3-D) Integration Technology

- EU FP7, 2007-2010
- 3D Network and Memory Architecture
- Partners: CEA LETI, Lancaster University, Hyperstone, Numonyx
- Main Results so far:
  - ⋆ 3D Router design
  - ⋆ 3D Architecture and Design space exploration

Current Group Activities

- 4 Faculty, 10 PhD students
- NoC PCB emulation platform
- Memory and Data management
- Performance Analysis
- Resource Allocation and Dimensioning for QoS
- Power Management
- Clocking and Synchronization
- 3D Architectures
- Circuit switched NoC
- Fault tolerance

Summary of Nostrum Status

- Nostrum defines a 2 D mesh topology;
- Protocol stack for link layer, network layer and session layer;
- Packet switched and virtual circuit communication services;
- Buffer-less, loss-less switch with no routing tables;
- 2 level data protection scheme;
- QoS Features;
- Programmable Data Management Engine
- Flexible NoC Simulator;

Ongoing Work:

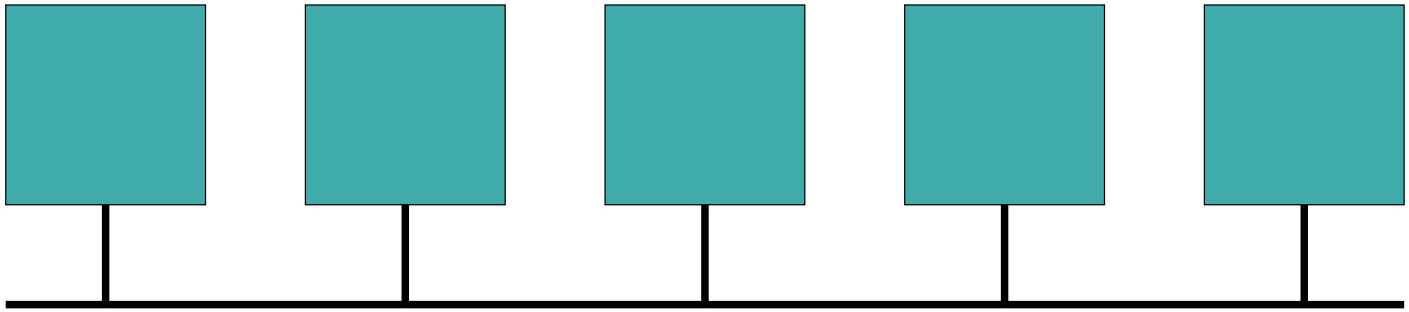
- Contract based QoS Provision
- Distributed Memory Architecture
- 3D Architectures
- Circuit switching network
- Fault tolerant NoC

Further information: www.ict.kth.se/nostrum

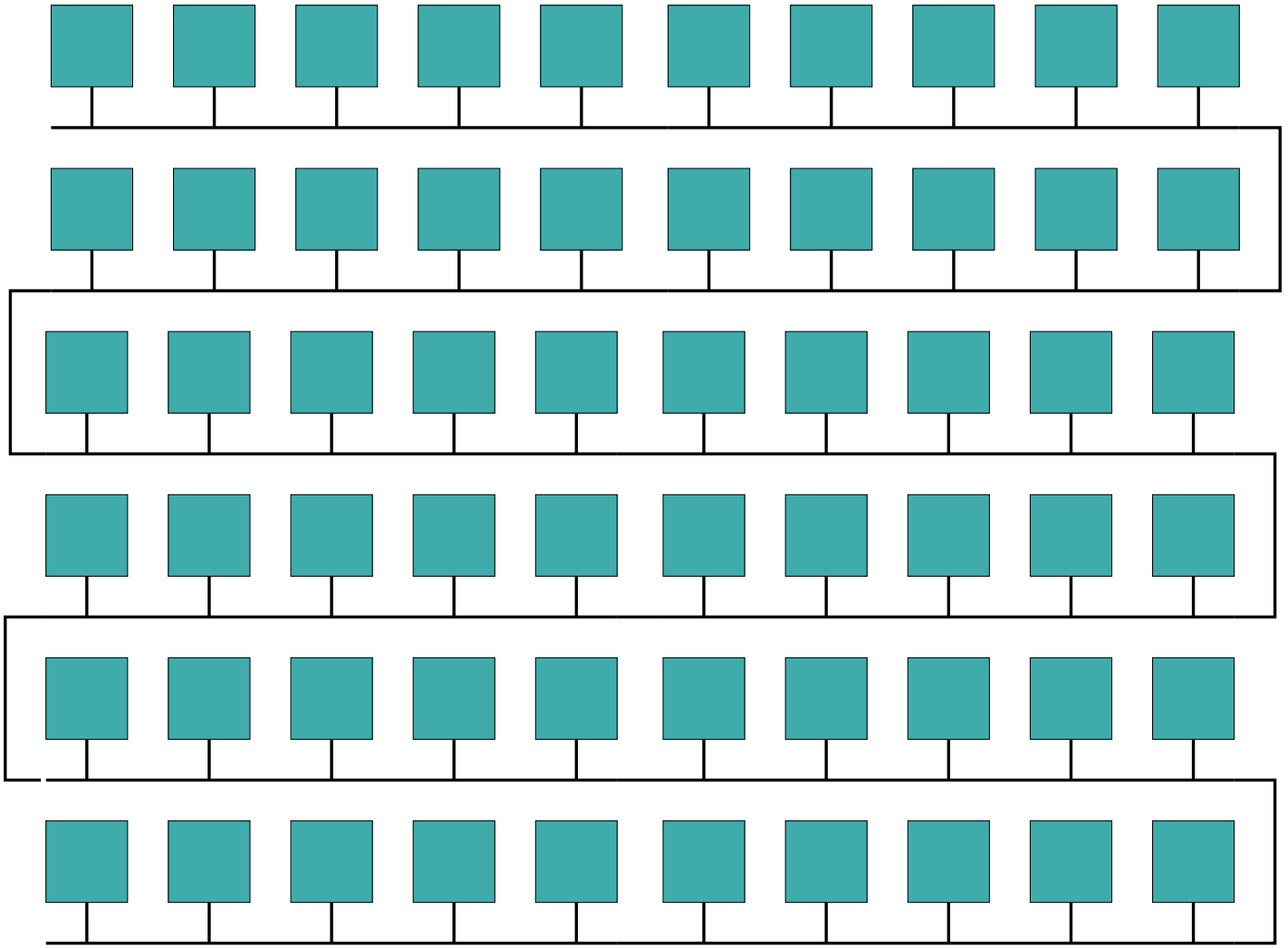
Network on Chip

- Topology
- Routing
- Switching
- Flow Control

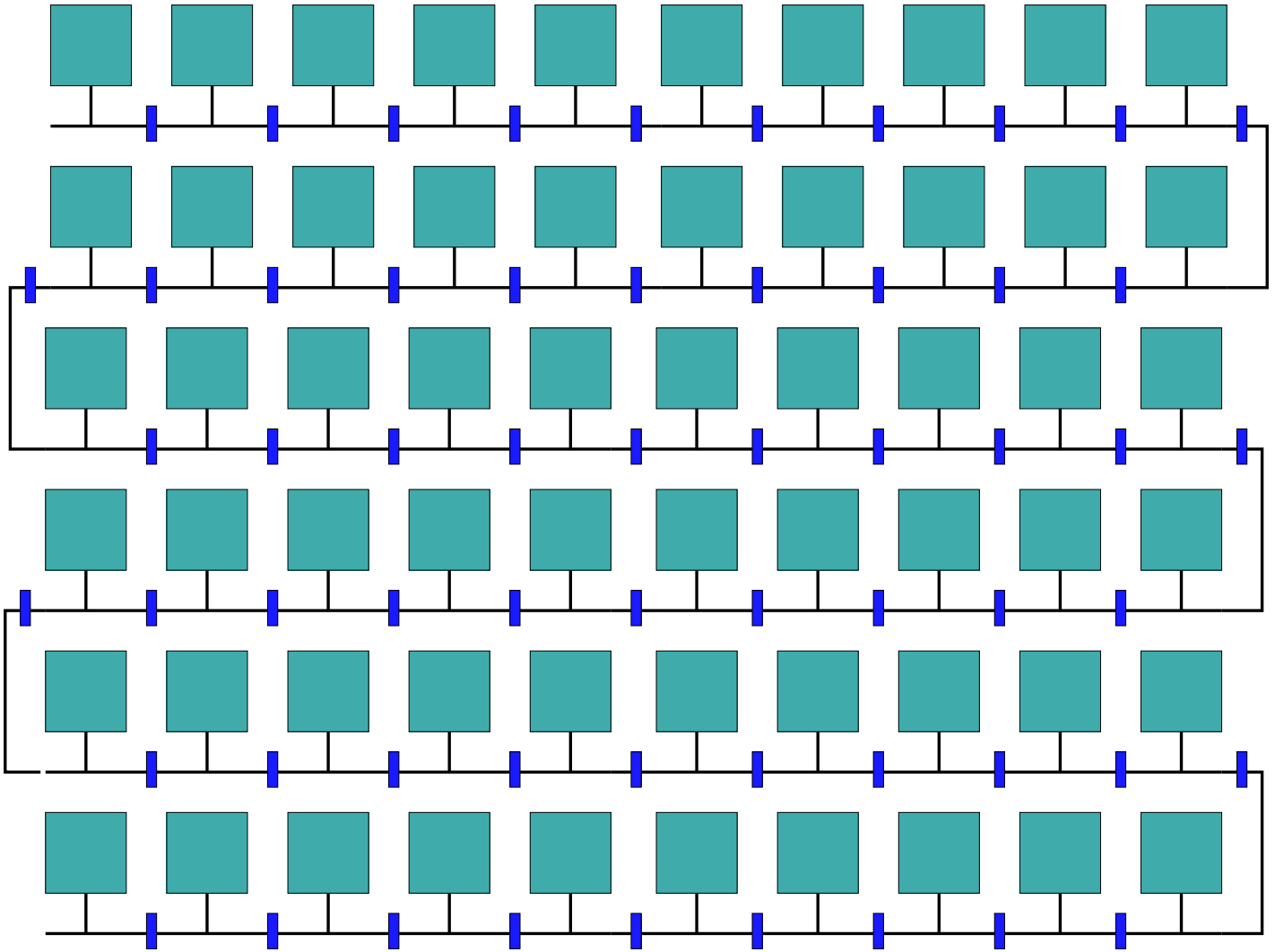
Buses are Efficient



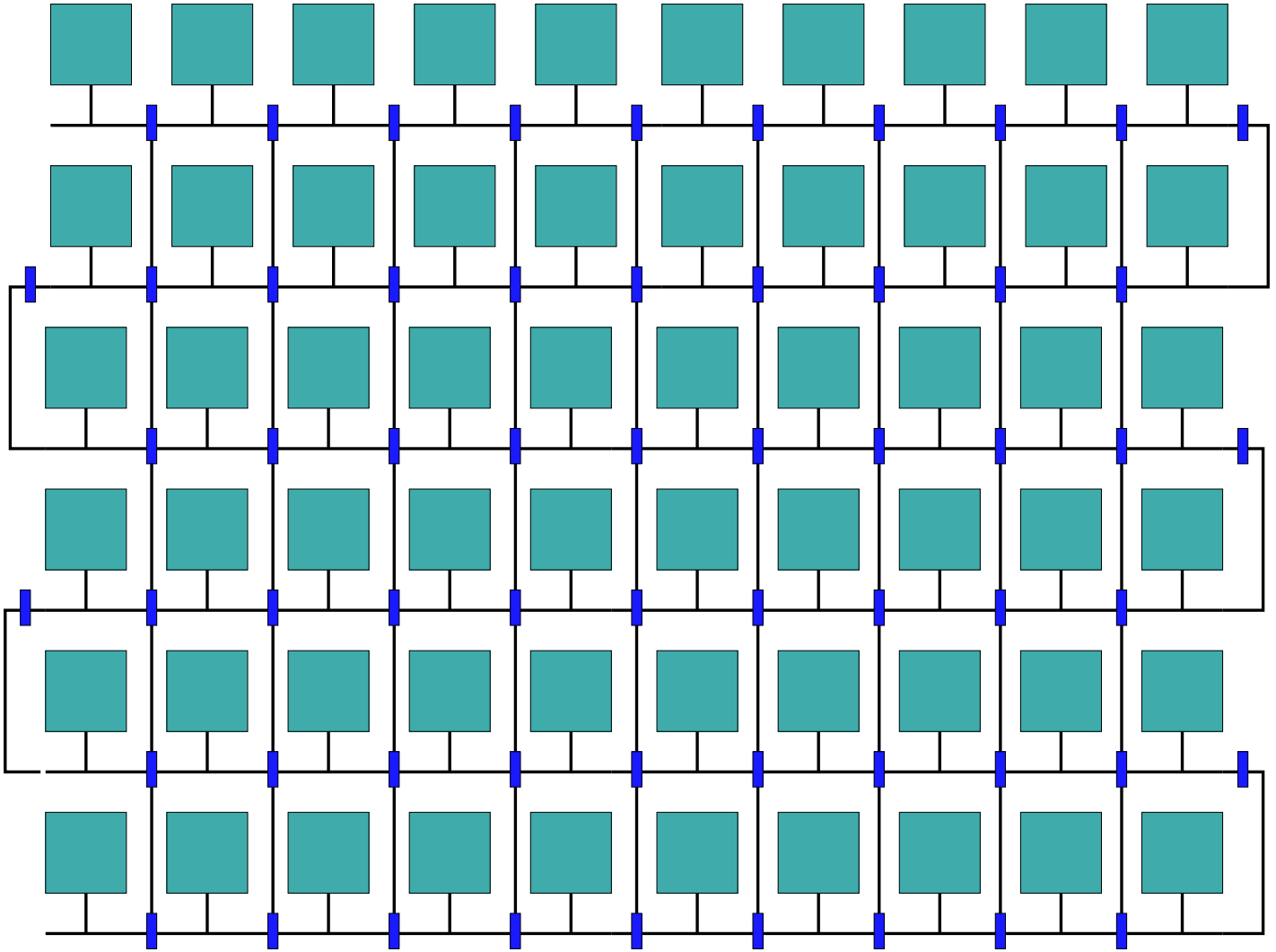
Buses Don't Scale



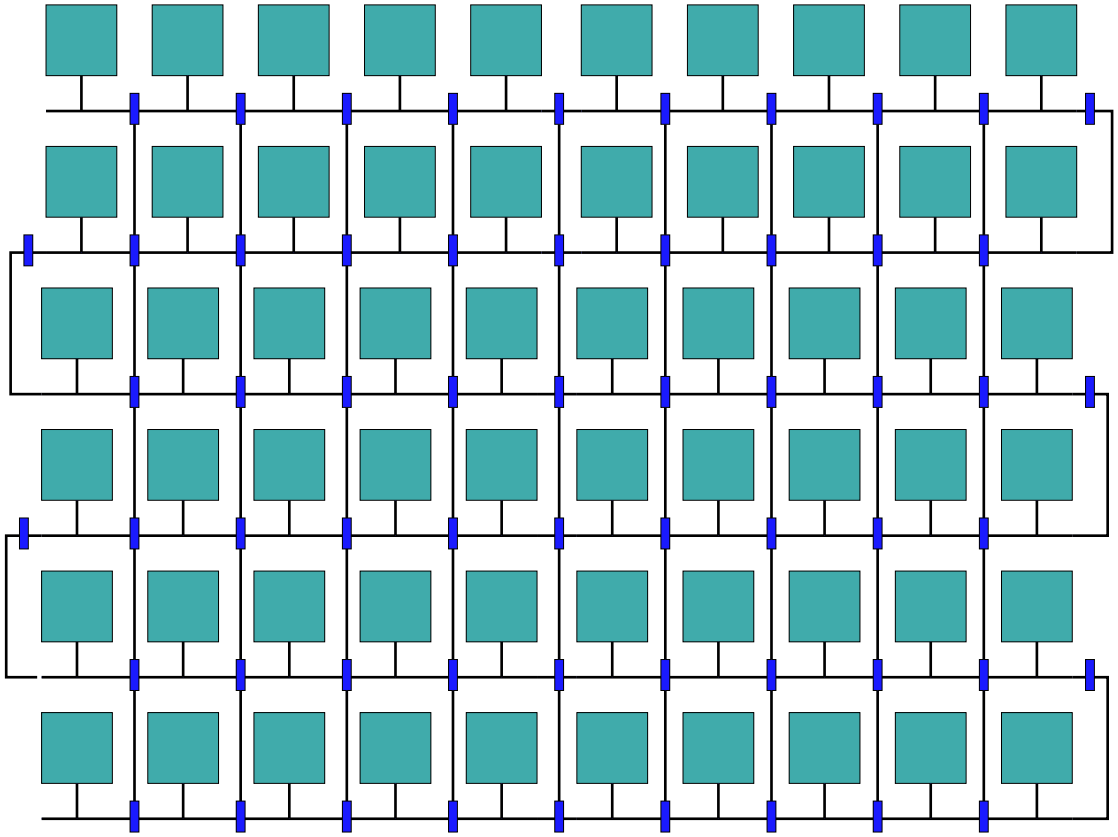
Bus + Pipelining



Bus + Pipelining + Parallelism

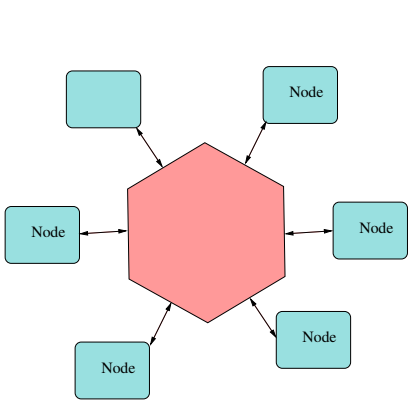


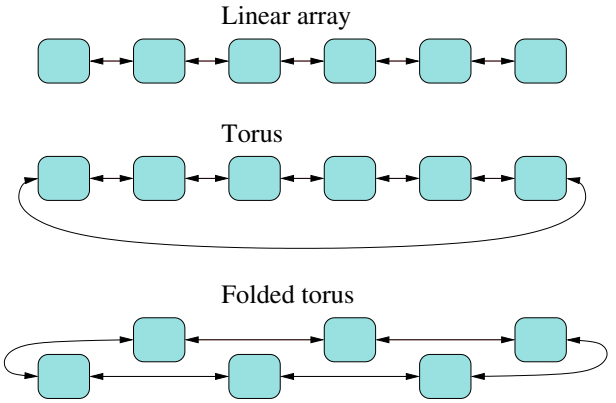
NoC Topics Overview

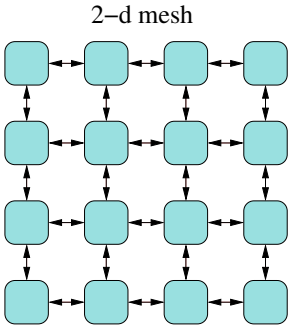


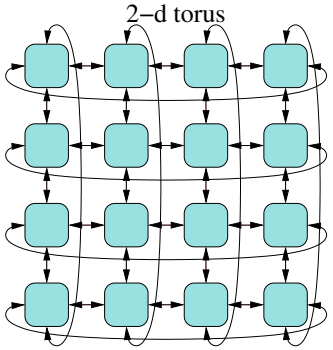
- Topology: How switches and nodes are connected
- Routing algorithm: Determines the route from source to destination
- Switching strategy: How a message traverses the route
- Flow control: What to do in the case of contention

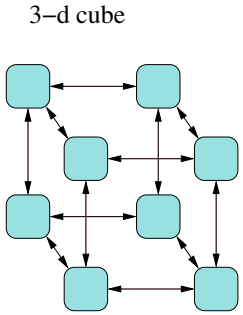
Topology

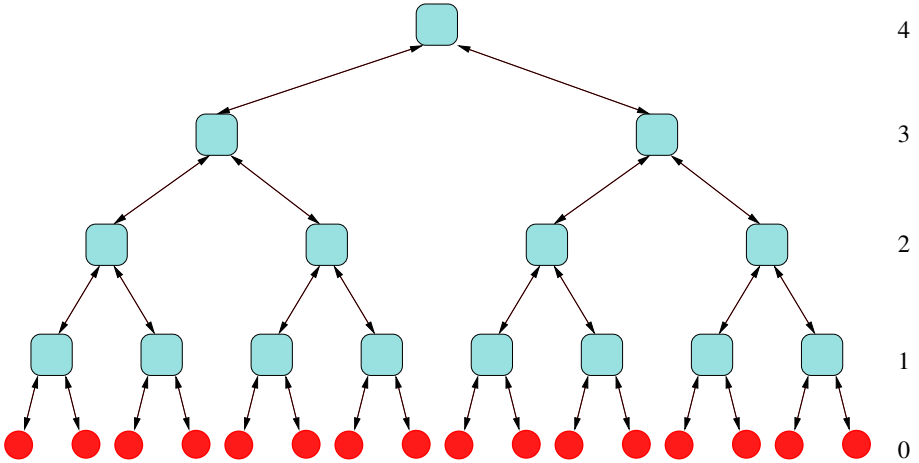

Node
Node
Node
Node
Node


Linear array
Torus
Folded torus

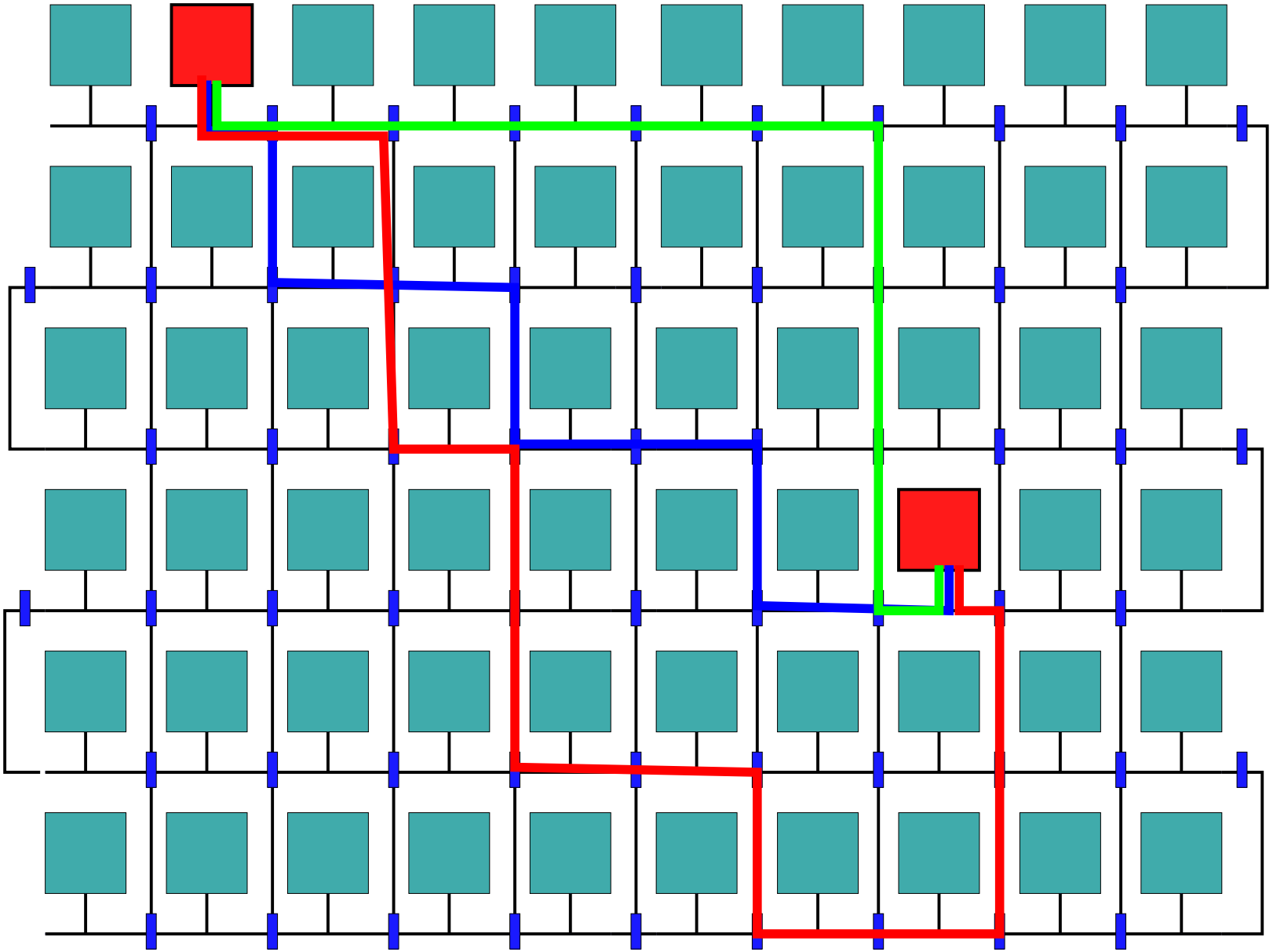

2−d mesh


2−d torus


3−d cube

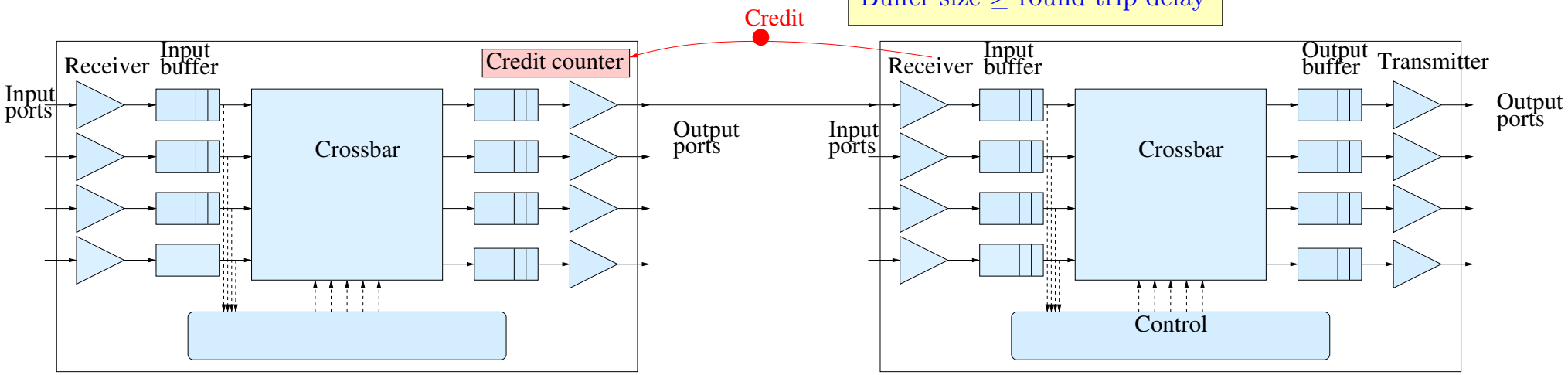

4
3
2
1
0

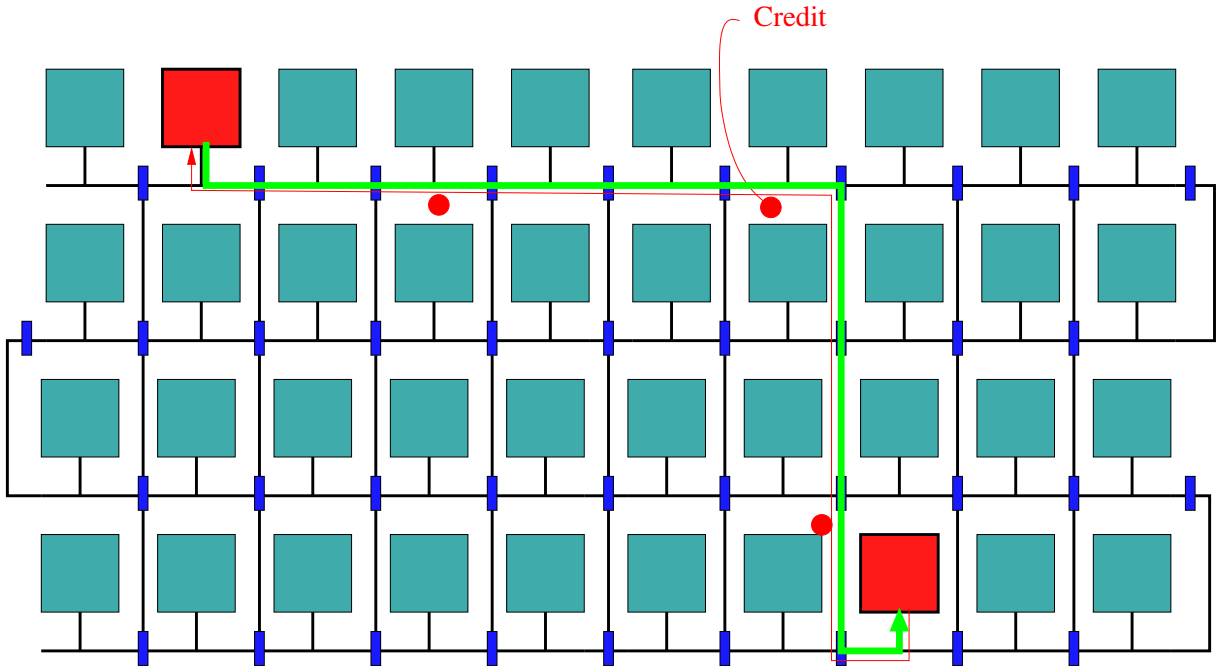
Routing



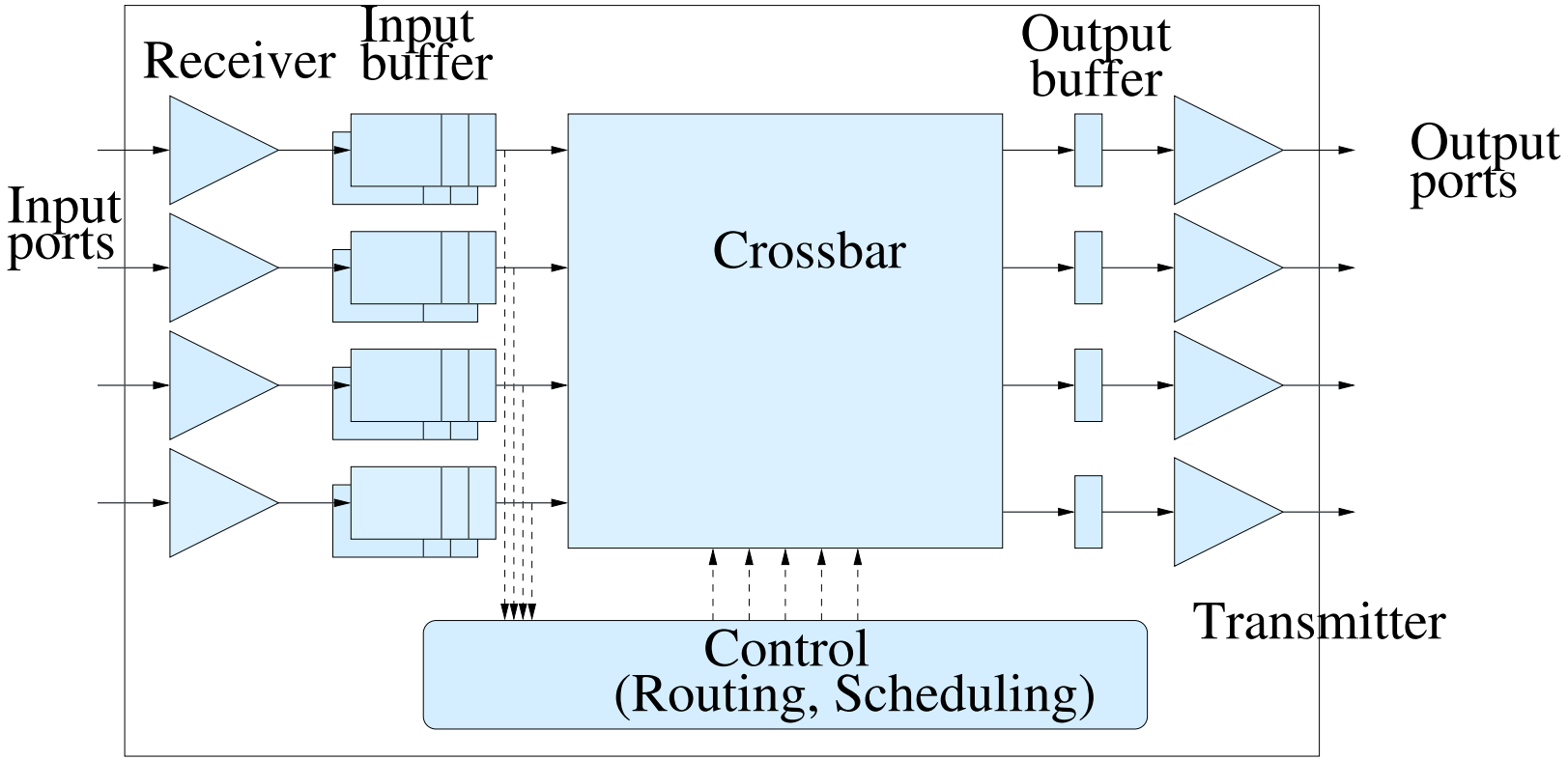
Flow Control

Buffer size $\geq$ round trip delay





Switching



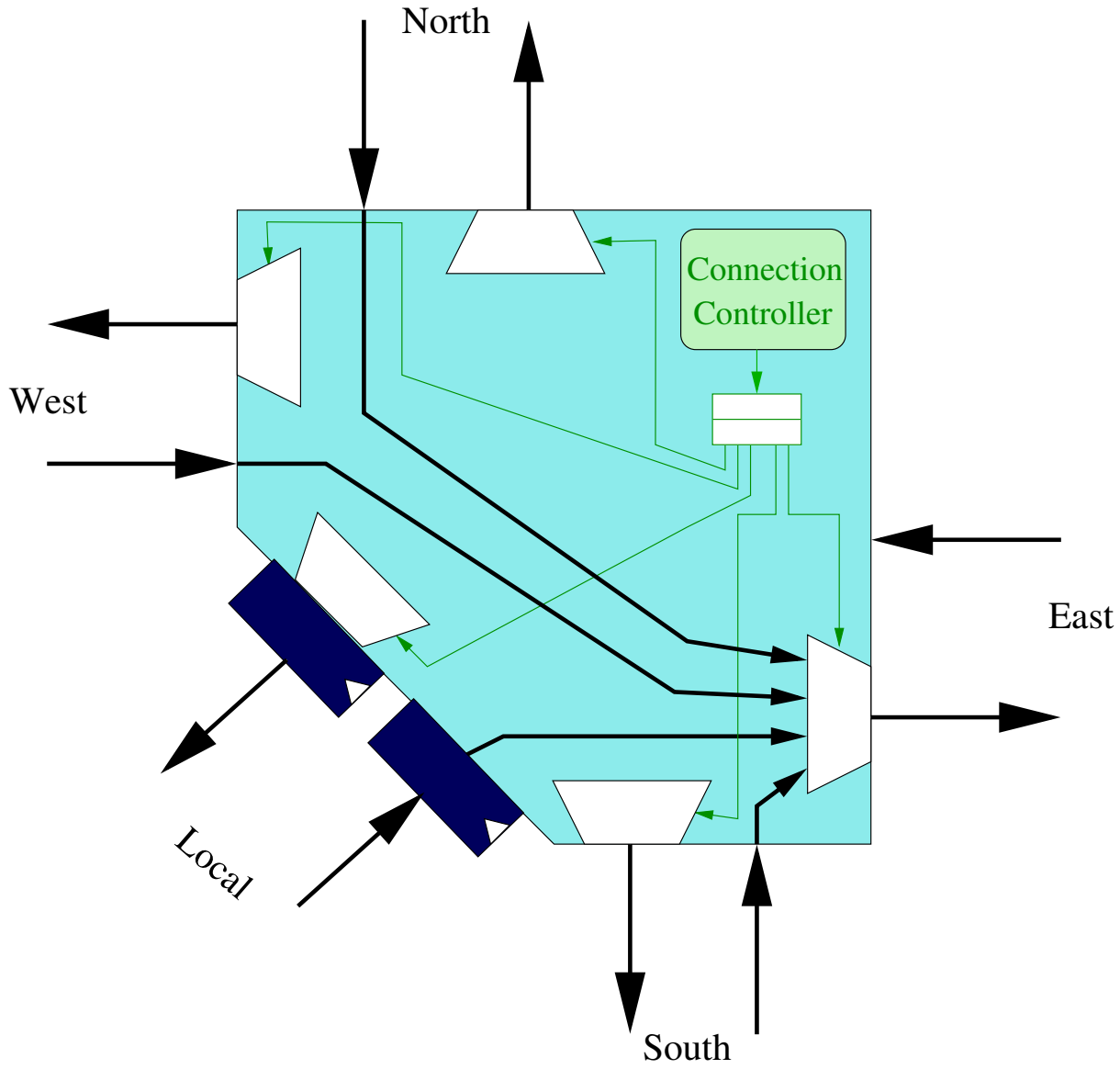
- Store & Forward
- Cut Through
- Wormhole

- Packet Switching
- Circuit Switching

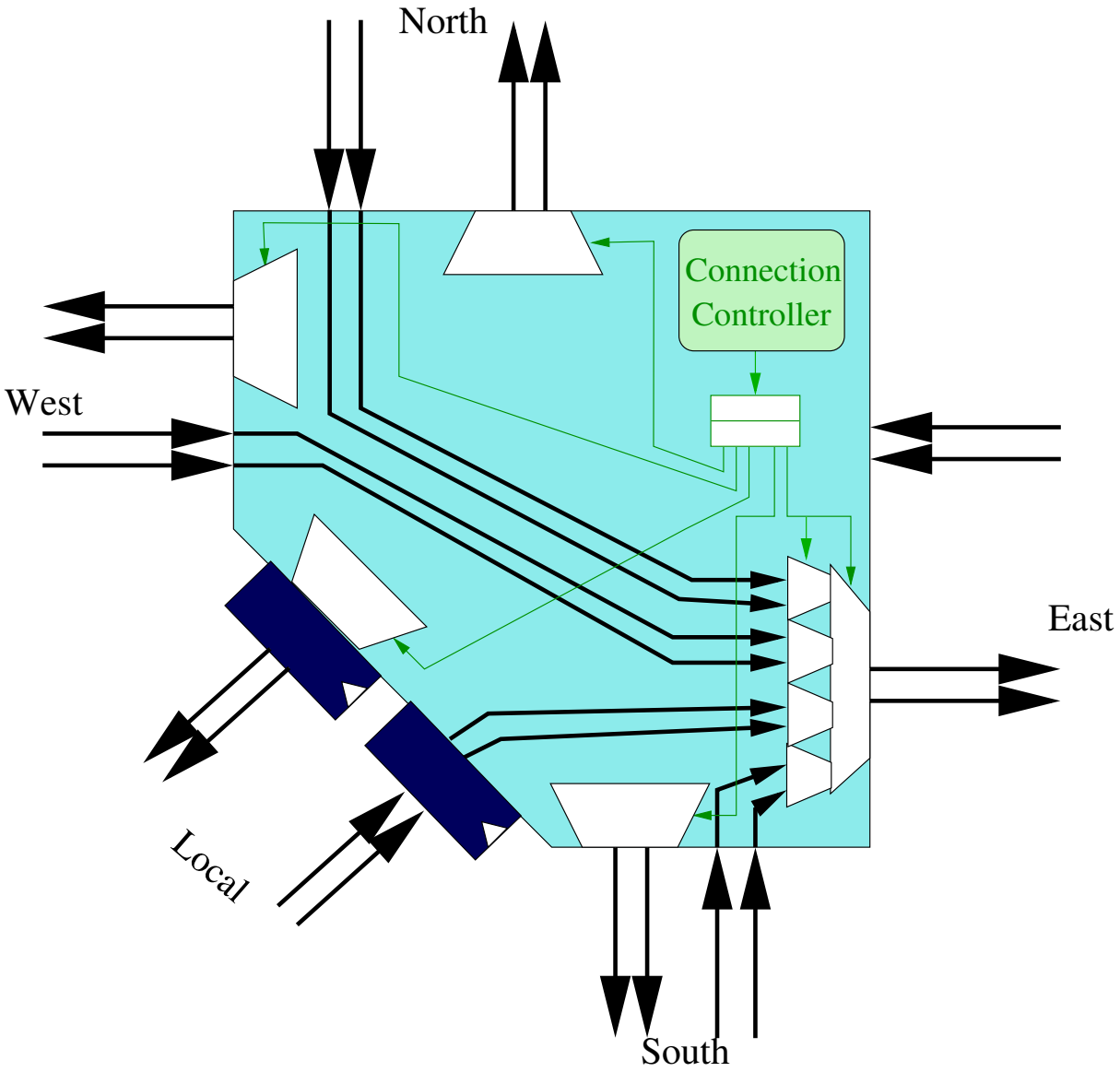
Circuit Switching

- Phases:
  - ⋆ Circuit Setup
  - ⋆ Transmission
  - ⋆ Tear Down
- Disadvantages:
  - ⋆ Exclusive allocation of resources
  - ⋆ Long setup phase
- Advantages:
  - ⋆ High performance - throughput and latency
  - ⋆ Low power consumption
  - ⋆ Low overhead during transmission phase
  - ⋆ Predictable transmission

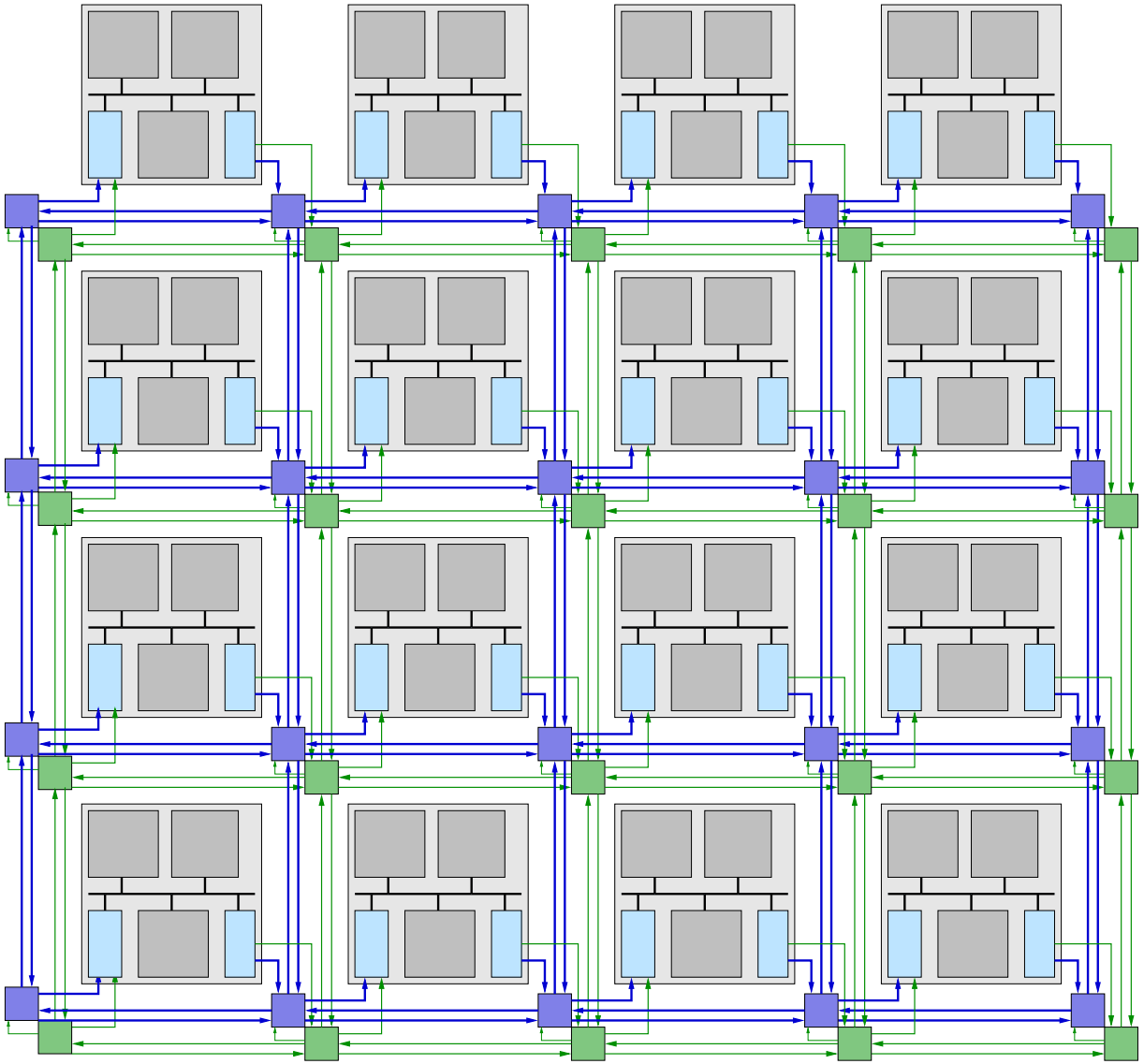
Circuit Switched Router



Spatial Division Multiplexing



Mixed NoC with Several Networks



Packet Switching vs Circuit Switching

	8×8		32×32	
	packet	circuit	packet	circuit
WC delay	56ns	7ns	248ns	31ns
Av delay	21ns	2.7ns	85ns	10.7ns
P2P bandwidth	54 Gb/s	127 GB/s	50 Gb/s	127Gb/s
Aggr. bandwidth	12 Tb/s	14 Tb/s	198 Tb/s	251 Tb/s

Packet Switched Network: 500MHz, 128 bit link

Circuit Switched Network: 1GHz, 128 bit link

Conclusions

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  but not in every combination
- The application characteristics are key in designing appropriate NoCs