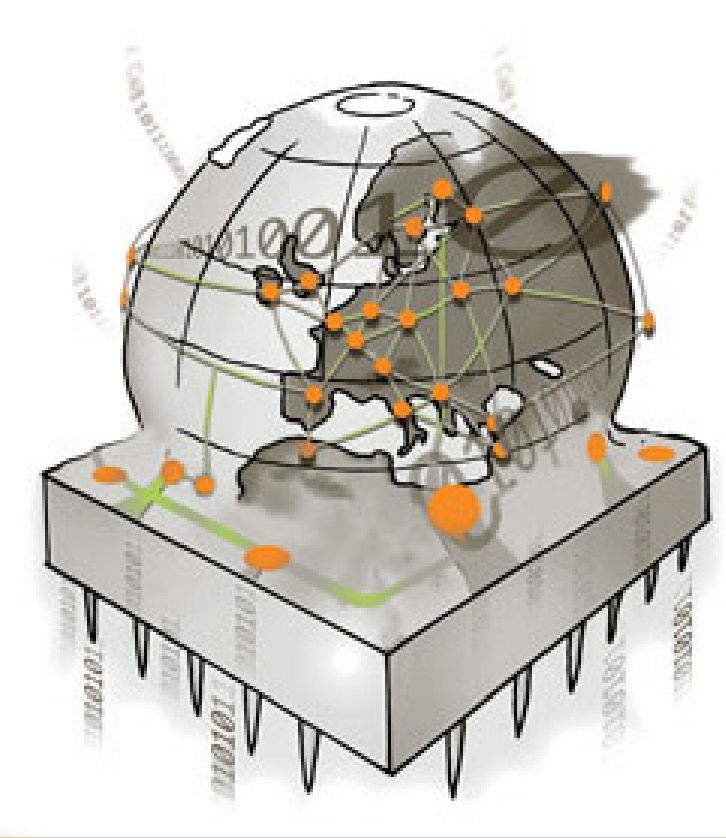
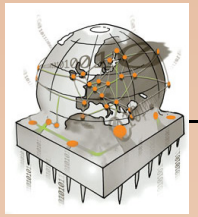
Networks on Chip



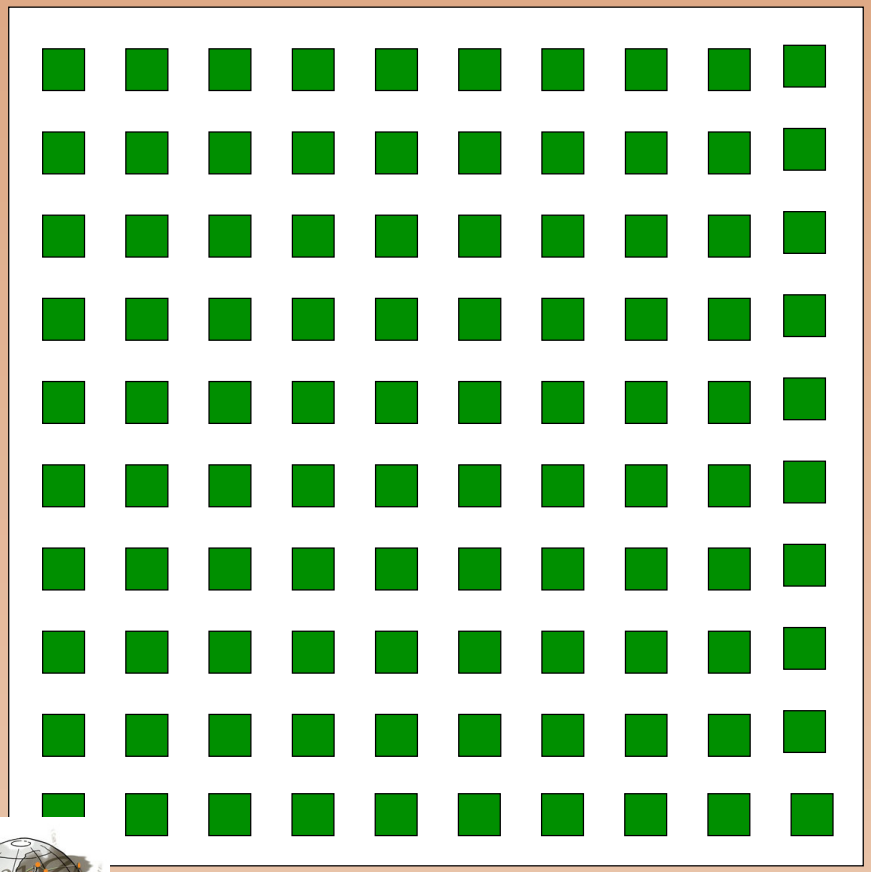
Shashi Kumar	Jönköping University
Ahmed Hemani	Spirea AB
Martti Forsell	
Juha-Pekka Soininen	VTT
Kari Tiensyrjä	
Li-Rong Zheng	
Hannu Tenhunen	
Axel Jantsch	Royal Institute
Mikael Millberg	of Technology
Johnny Öberg	

Overview

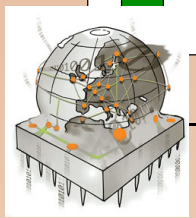
- Part I: Introduction, Axel Jantsch, KTH
- Part II: Physical Issues in NOCs, Li-Rong Zheng, KTH
- Part III: Introduction to concepts in parallel computing, Martti Forsell, VTT
- Part VI: NOC Architecture, Axel Jantsch, KTH
- Part V: A NOC Design Methodology, Juha Pekka Soininen, VTT



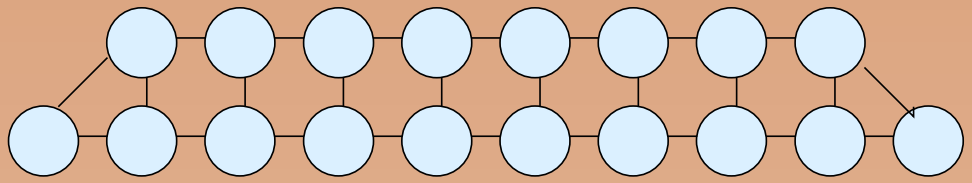
The Challenge



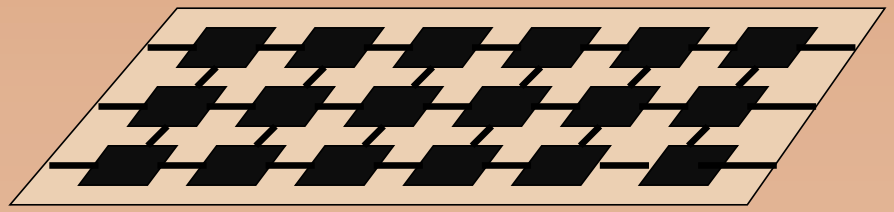
# Gates	# Processors	Year
6 M	4	2000
24 M	16	2003
96 M	64	2006
384 M	256	2009



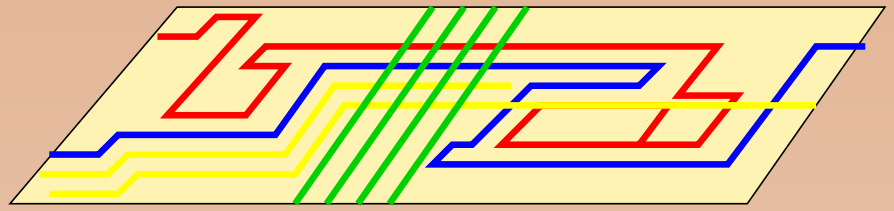
Functions, Architecture, and Physics



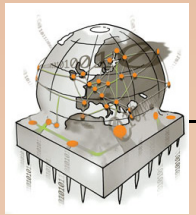
Concurrent processes



Large number of resoucres

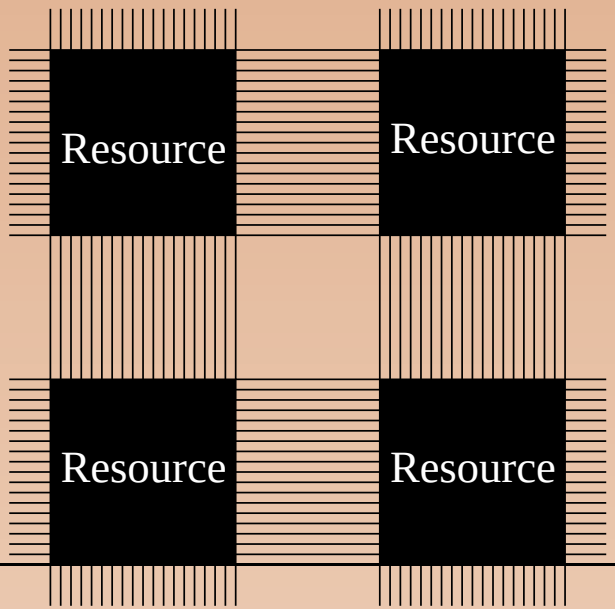


Physical issues



Challenge Areas: Physical Issues

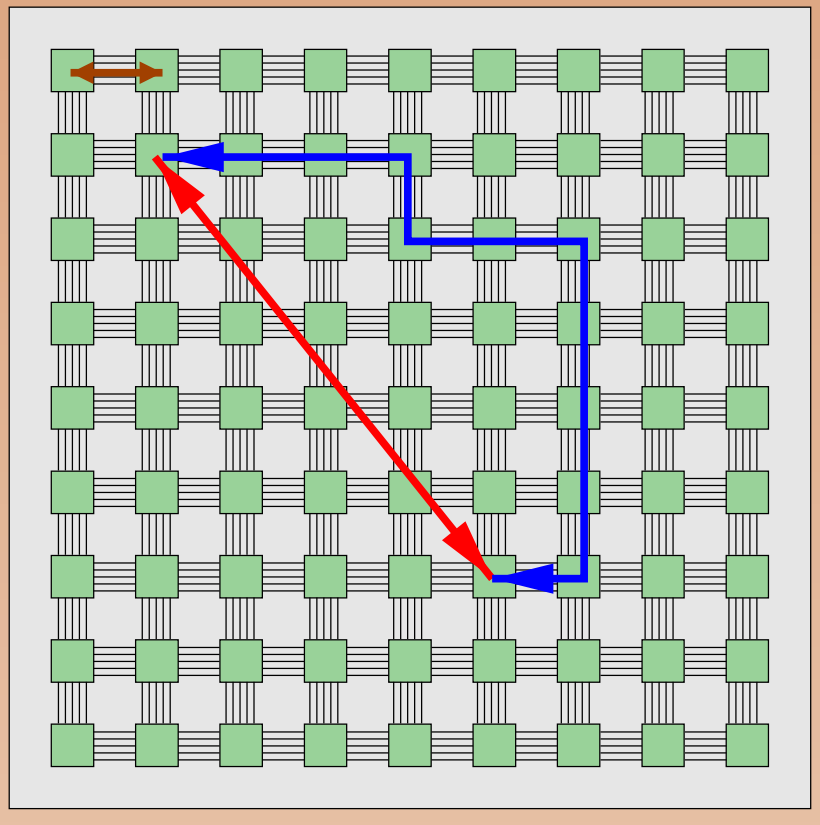
- Deep submicron effects, noise, signal integrity
- Interconnect
- Power consumption, power delivery
- Clock distribution
- Memory integration (50-80% of the chip)



Scenario:

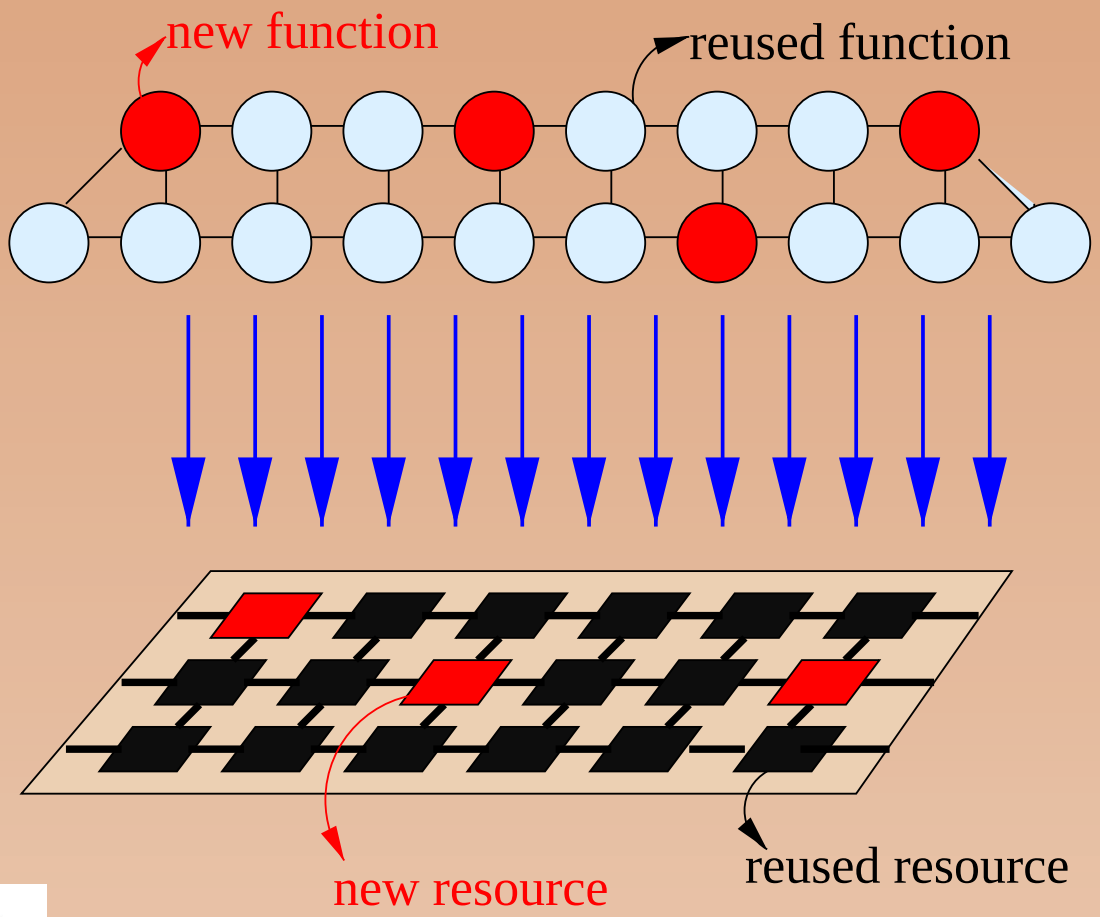
- 60 nm CMOS
- 22×22 mm Chip size
- 2×2 mm resource size
- 300 nm minumum wire pitch
- 6600 wires between two resources on each metal layer

Challenge Areas: Architecture



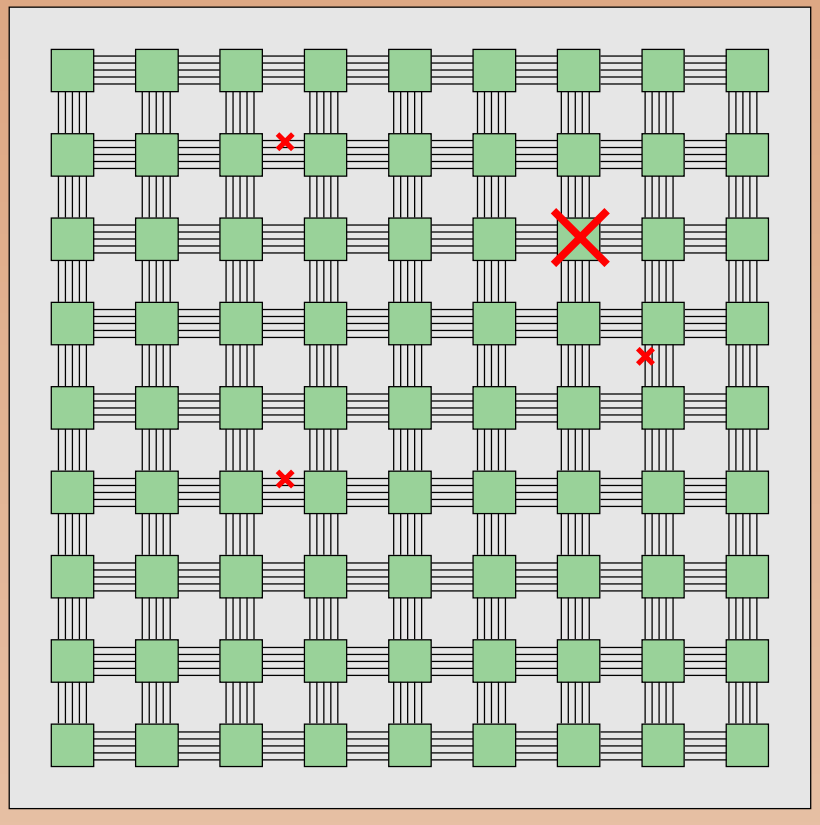
- Communication infra-structure
  - ⋆ Physical layer
  - ⋆ Data link layer
  - ⋆ Network layer
  - ⋆ Transport layer
- Type and size of resources (Micro processor, DSP, memory, FPGA, etc.)
- Resource usage

Challenge Areas: Methodology



- Specification techniques of concurrent activities
- Performance analysis
- Reuse and Integration of both functions and components

Challenge Areas: Run Time Services

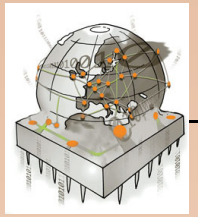


- Monitoring
- Fault-tolerance,
- Diagnostics
- Fault recovery
- Dynamic resource management

Challenge Areas: Configurability

A sensible trade-off between efficiency and generality is critical.

- Configurability of communication resources from the data link to the application layer
- Configurability of resources (processors, DSPs, FPGAs, etc.)
- When and who?
  - ⋆ Design-time configuration: Platform ⇒ Pruduct
  - ⋆ Static product configuration: Once for a product
  - ⋆ Dynamic reconfiguration: Programming of the product



References

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[2] Ahmed Hemani, Axel Jantsch, Shashi Kumar, Adam Postula, Johnny Öberg, Mikael Millberg, and Dan Lindqvist. Network on chip: An architecture for billion transistor era. In *Proceeding of the IEEE NorChip Conference*, November 2000.

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[4] Drew Wingard. MicroNetwork-based integration of SOCs. In *Proceedings of the 38th Design Automation Conference*, June 2001.

[5] Henry Chang, Larry Cooke, Merrill Hunt, Grant Martin, Andrew McNelly, and Lee Todd. *Surviving the SOC Revolution - A Guide to Platform-Based Design*. Kluwer Academic Publishers, 1999.

[6] Network on Chip: A Novel Architecture Template for Integrated Telecommunication Systems http://www.ele.kth.se/NOC/