Memristors' Potential for Multi-bit Storage and Pattern Learning

Nima TaheriNejad, Sai Manoj P. D., and Axel Jantsch
Institute of Computer Technology
Faculty of Electrical Engineering and Information Technology
Technische Universität Wien (Technical University of Vienna)
Gusshausstrasse 27-29, 1040 Vienna, Austria
Email: {nima.taherinejad, sai.dinakarrao, axel.jantsch}@tuwien.ac.at

***Abstract*—Memristor is a two-terminal device, termed as fourth element, and characterized by a varying resistance depending on the charge (current) flown through it. This leads to many interesting characteristics, including a memory of its past states, demonstrated in its resistance. Smaller area and power consumed by memristors compared to conventional memories makes them a more suitable choice for applications needing large memory. In this paper we explore one of the unique properties of memristors which extends their suitability by allowing storage of multi-bit data in a single memristor. Their ability of storing multi-bit patterns will be shown via a simplified proof and simulations. This characteristic can be advantageous for many applications. In this paper particularly, we briefly discuss its advantages in pattern learning applications.**

***Keywords*—Memristors; Multi-bit Storage; Pattern Learning; Pattern Recognition; Precision; Digital Coding Systems**

I. Introduction

Memristor [1]–[4] is a two terminal non-volatile memory device based on resistance switching. It is termed as the fourth element [2], and is characterized by the constitutional relation between charge (q) and flux (ϕ). In other words, a memristor is a device whose resistance varies depending on the current (charge) that has flown through it.

Memristors can be built from various materials and have different operating characteristics. However, a distinctive fingerprint characteristic of all memristors is exhibiting a pinched hysteresis loop behavior. For every different input pattern, memristor reaches a different point on the hysteresis loop (Fig. 1). This can be taken advantage of, in order to differentiate inputs as well as to learn or identify the input patterns. Particularly, power consumption of memristors have been reported to be smaller compared to the existing memory devices [5], [6]. This makes them a suitable choice for several applications in need of large memories, specially if they are battery powered. A distinct case of such applications is pattern learning and recognition. Pattern learning and recognition is one of the key aspects in biological systems [7], [8]. Therefore, it has attracted a significant interest from researchers for implementation of similar non-biological systems [7]. In general, patterns are unique, but are composed of smaller segments, which repeat and occur in a random manner. Storing individual segments, or as a group, in a conventional memory requires a large amount of storage. To alleviate the need for large memories, some techniques such as encoding techniques [9] have been proposed. However these techniques require considerable pre- and post-processing to encode and decode the data.
Alternatively, using memristors to store the patterns can reduce the required memory, area and power as well. In addition, memristors have a characteristic of learning at the basic level, i.e., memorizing the sequence and providing the output based on the current state and inputs. This behavior helps in adapting to the environment more efficiently. However, this paper focuses on the state transition (variation of resistance) with inputs and differentiating the inputs based on the reached states (resistance values).

The rest of this paper is organized as follows: First, we briefly review the basic principles of memristors in Section II. Next, in Section III, we present our hypothesis on a characteristic of memristors which can lead to multi-bit storage. We support that claim with a simplified proof for the hypothesis. Then, we discuss how the proposed property can be used in real applications such as multi-bit data storage and pattern learning. In the next section, Section IV, we present and discuss our simulation results. And finally we point out some potential future works and conclude the paper in Section V.

II. Memristors: A brief review

In 1971, Leon Chua proposed the theory behind memristors, i.e. the relation between flux and charge [1], [3]. In this paper memristor is mentioned as the fourth element along side with resistors, inductors and capacitors [1], [3]. In practice however, the fourth element did not come about until 2008,

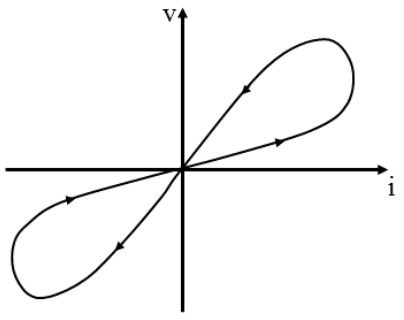

Fig. 1. Voltage of a memristor as a function of the current going through it.

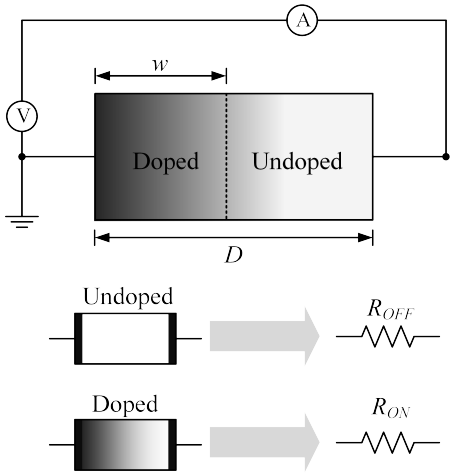

Fig. 2. Memristor built as a doped-undoped semiconductor structure.

when HP fabricated the first memristors [2]. By now, memristors have been used for building Look-Up Tables (LUTs) [10], sequential logic operations [11], transistors [12] and other fundamental operations [8], [13]. They are being increasingly considered and used for more and more applications [9]. In the same light, in this paper we will explore their potential as a multi-bit storage unit that could be considerably beneficial to applications such as pattern learning and recognition. However, before delving into the respective details, first, we briefly review the construction of these devices in this section. Then, we study the physics of these devices and formulate the equations describing their behavior. These two subsections will lay the foundation for our hypothesis, proof and discussion in the next sections.

A. Device Construction

Memristor is a two terminal device made out of semiconductor material sandwiched between the two ends. A portion of the semiconductor material is doped and the rest of the structure is undoped (Fig. 2, top). With the application of a voltage, the boundary region between the doped and undoped regions drift. This leads to a lower resistance with the application of a positive voltage, and a higher resistance with a negative voltage. It needs to be noted that the boundary of doped and undoped regions changes only at the application of external voltage. This makes the device non-volatile.

B. Memristance

Memristance of the device shown in Fig. 2 can be calculated by [2]

$$R = R_{\text{on}}\frac{w}{D} + R_{\text{off}}(1 - \frac{w}{D}), \tag{1}$$

where R_{on} and R_{off} are the minimum and maximum resistance, respectively. D is the length of the semiconductor device and w is the width of doped area as a function of current, given by [4]

$$\frac{dw(t)}{dt} = k_m W(w) I, \tag{2}$$

where k_m is a constant and $W(w)$ is a window function often selected as [14]

$$W(w) = 1 - (2w - 1)^{2p}, \tag{3}$$

where p is a positive integer related to switching linearity. Devices with higher switching linearity can be modeled by larger p values. Changes of the width (w) -namely the boundary drift- can have different effect which should be modeled differently for various types of memristor. Some of these different memristors and their models can be found in [4]. In this paper, following [4], we consider a $W(w)$ with $p = 1$, which leads to an expression for w as a function of charge (q);

$$\frac{1}{4} ln \frac{w}{1 - w} = k_m(q(t) + q_0), \tag{4}$$

where q_0 is the initial condition. By plugging Eq. (4) into the Eq. (1), we have [4]

$$R(q(t)) = R_{\text{off}} + \frac{R_{\text{on}} - R_{\text{off}}}{e^{-4k_m(q(t)+q_0)} + 1}. \tag{5}$$

III. Hypothesis and Simplified Proof

As established in the literature, the resistance of memristor depends on its current state (charge). For this study, we have selected and used the ideal memristor model given by Eq. (5) [4].

A. Hypothesis

Claim: *Not only the resistance of memristor depends on its current state, but also the changes of resistance depends on its current state.*

In other words, applying two instances of the same signal to a memristor at different states, will produce a different effect in changes of resistance. The difference between the amount of change in resistance depends on the respective state of the memristor. Particularly, each pulse in a series of pulses applied to a memristor will produce different changes of resistance. This makes each pulse unique, according to its turn in the pulse-train.

B. Problem Elaboration

Consider two pulses -A and B- with the same voltage and time length, applied to a memristor at different states. Since different states means different resistances, the value of the current going through the memristor due to each pulse will be different:

$$\Delta q_{\text{A}}(R_{\text{A}}) \neq \Delta q_{\text{B}}(R_{\text{B}}) \tag{6}$$

This in turn leads to different changes of charge in the memristor. However, as Eq. (5) states, changes of resistance is in a non-linear relation with changes of charge. In other words, even if the applied charges were equal, it would not mean similar resistance changes.

$$\Delta q_{\text{A}} = \Delta q_{\text{B}} \implies \Delta R_{\text{A}} = \Delta R_{\text{B}} \tag{7}$$

Furthermore, we should consider that even within a pulse window, the resistance of the memristor changes according to Eq. (5). Therefore, the changes in the charge flow are not linear either and depend upon the changes of resistance of the memristor. In other words:

$$dq_x = f(dR_x), \tag{8}$$

where $x \subset \{A, B\}$ and f could be derived from Eq. (5).

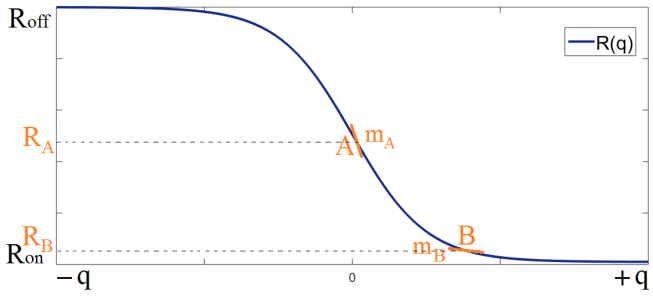

Fig. 3. Resistance of the ideal memristor as a function of the charge stored in it.

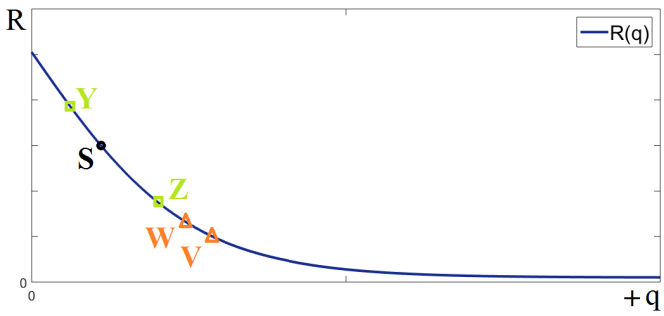

Fig. 4. Change of state in memristor, according to the pattern of input pulse.

Therefore the objective of this section is to show that the changes of resistance due to similar input pulses are different at different states of memristor;

$$dR_{\mathrm{A}} \neq dR_{\mathrm{B}}, \tag{9}$$

and preferably to estimate

$$\frac{dR_{\mathrm{A}}}{dR_{\mathrm{B}}}. \tag{10}$$

C. Simplified Proof

Following the flow of the previous subsection, the first step is to calculate the amount of charge applied to the memristor at each instance due to the respective pulse. Once we know the changes in the charge we can calculate the changes in resistance as well. However, the current and hence the applied charge depends also on the changes of resistance within the time frame. To simplify this inter-dependency we assume the time-window to be small enough such that we can assume the resistance changes are linear within that window. In other words,

$$R(q) = -m_x q + R_x, \tag{11}$$

where m_x is the slope of the Eq. (5) at point $x \subset \{A, B\}$. This is shown graphically in Fig 3.

Therefore based on Ohm's law and the definition of current we have,

$$\begin{aligned} V = R\frac{dq}{dt} \rightarrow \quad & Vdt = Rdq = (-m_x q + R_x)dq \\ \rightarrow \quad & \int_0^T V dt = \int_0^{dq_x} (-m_x q + R_x)dq \\ \rightarrow \quad & VT = \tfrac{-m_x}{2}(dq_x)^2 + R_x dq_x. \end{aligned} \tag{12}$$

where T is the pulse-width and V is the voltage of the applied pulse.

Solving Eq. (12) for dq_x we have

$$dq_x = \frac{R_x}{m_x} K_x, \tag{13}$$

where

$$K_x = 1 + \sqrt{1 - \frac{2m_x VT}{R_x^2}}. \tag{14}$$

Now referring to Eq. (11), we have

$$\frac{dR_x}{dq_x} = -m_x. \tag{15}$$

By combining Eq. (13) and Eq. (15) we have

$$\begin{aligned} &\frac{dR_{\mathrm{A}}}{dq_{\mathrm{A}}} \Big/ \frac{dR_{\mathrm{B}}}{dq_{\mathrm{B}}} = \frac{m_{\mathrm{A}}}{m_{\mathrm{B}}} \rightarrow \frac{dR_{\mathrm{A}}}{dR_{\mathrm{B}}} \frac{dq_{\mathrm{B}}}{dq_{\mathrm{A}}} = \frac{m_{\mathrm{A}}}{m_{\mathrm{B}}} \longrightarrow \\ &\frac{dR_{\mathrm{A}}}{dR_{\mathrm{B}}} = \frac{m_{\mathrm{A}}}{m_{\mathrm{B}}} \Big(\frac{R_{\mathrm{A}} K_{\mathrm{A}}}{m_{\mathrm{A}}} \Big/ \frac{R_{\mathrm{B}} K_{\mathrm{B}}}{m_{\mathrm{B}}} \Big) \rightarrow \frac{dR_{\mathrm{A}}}{dR_{\mathrm{B}}} = \frac{R_{\mathrm{A}} K_{\mathrm{A}}}{R_{\mathrm{B}} K_{\mathrm{B}}}. \end{aligned} \tag{16}$$

However, since wherever m_x is large, R_x is also very large and vice-versa, typically the last term in Eq. 14 is significantly smaller than one[1]. In other words, $K_x \approx 2$, which leads to

$$\frac{dR_{\mathrm{A}}}{dR_{\mathrm{B}}} \approx \frac{R_{\mathrm{A}}}{R_{\mathrm{B}}}. \tag{17}$$

Therefore, change of resistance of a memristor due to a pulse at point A, compared to the resistance change due to the same pulse at point B, is proportional to the ratio of the resistance of the memristor at the respective points.

D. Application

In order to use this property, let us consider a memristor at state S, as shown in Fig. 4. We would like to study the effect of a simple pulse train on the changes of state in the memristor.

1) Case "10": Assume that when a positive pulse, representing the logical value of "1", is applied to the memristor, it moves to state V. Now, if a second pulse which is negative, representing the logical value of "0", is applied to the memristor, it moves to the new state of W.

2) Case "01": Assume that first pulse is negative ("0") and changes the state of memristor to Y. Let us consider that the second pulse is positive ("1") and changes the state of memristor to Z.

3) Analysis: The question is whether the two states, W and Z, are the same or are they different?

In response we should consider that the forward movement, SV depends on R_S, whereas YZ movement depends on R_Y. In that case, assuming that the conditions are met for Eq. (17) to hold, we have

$$\frac{SV}{YZ} = \frac{R_S}{R_Y}. \tag{18}$$

[1] For example in the instance of memristor we use in this study, $m_{\max} \approx 0.0099$, the smallest value of memristor resistance ($R_{\mathrm{on}} = 100$), and the product of maximum voltage and pulse-width ($VT_{\max} \approx 0.19$). This leads to the last term to be 3.76×10^{-7} which even though exaggerated, is yet several orders of magnitude smaller than one.

TABLE I. CHANGES OF STATES (RESISTANCE) IN A MEMRISTOR AS A 2-BIT STORAGE UNIT. PULSE WIDTH, $T = 0.25s$.

Pattern	Negative Pulse [V]		
	-0.25	-0.5	-0.75
	Resistance of Memristor [$k\Omega$]		
"00"	7.078	8.285	8.998
"01"	3.599	5.121	6.288
"10"	3.360	4.873	6.053
"11"	0.100	0.100	0.100

Similarly, for the negative pulses (backward movements), we have

$$\frac{SY}{VW} = \frac{R_S}{R_V}. \tag{19}$$

Combining these two equations we get

$$\begin{aligned} W &= SV - VW \\ Z &= -SY + YZ \\ \rightarrow Z &= -\frac{R_S}{R_V}VW + \frac{R_Y}{R_S}SV. \end{aligned} \tag{20}$$

Based on Eq (20), for an equal Z and W, we need $R_S = R_V$ and $R_Y = R_S$. However, since those resistances are different (three different states, caused by different inputs), we have $Z \neq W$. Therefore, the two states of W and Z are different and each represents a unique set of input; "10" and "01" respectively.

Once the input series leading to each state is identified, this information can be used to decode inputs of each memristor. Hence, this characteristic can be used to store a pattern or a multi-bit data in a single memristor cell.

IV. SIMULATIONS AND DISCUSSIONS

A. Simulation Set-up and Results

In order to evaluate this method of data storage, in this section we present the result of our simulations. Simulations were run on LTSpice and using the ideal model presented by [4] (seen in Eq. (5)). For the simulations we have used the following parameter values as given by [4]; $R_{\text{on}} = 100\Omega$, $R_{\text{off}} = 10k\Omega$, and $k_m = 10000$.

We have tested the memristor as two-bit and three-bit storage cell and the results are compiled in Table I and Table II, respectively. The results shown in Table I and Table II, correspond to the left to right order of input pulses. In other words, the memristor was supplied with the value of Most Significant Bit (MSB) first and the value of Least Significant Bit (LSB), last. This pattern leads to a uniform change of resistance in Table I corresponding to the binary values. Similar uniformity, with expected exception of the "100" case, is observed in Table II as well. In the next subsection, we will discuss this expected exception further.

Time-length of each pulse for the two-bit storage simulation was chosen to be $0.25s$. This would lead to early saturation[2] of memristor in the case of the three-bit storage scenario. This would result in indistinguishable states. Therefore, to avoid this phenomenon, for three-bit simulations pulse-width of $0.1s$ was used.

[2] Entering deeply into either region of $R = R_{\text{on}}$ or $R = R_{\text{off}}$, at the two ends of Fig. 3.

In all simulations we have used positive pulses with the voltage of $0.5V$, whereas for the negative pulses we explored the effect of three different values of voltage (namely, $-0.25V$, $-0.5V$, and $-0.75V$). In the case of two-bit storage, as it can be seen in Table I, the -0.25V produces the largest difference between various states. The difference of this effect is even larger once we consider the relative difference of the resistances. Interestingly in the case of three-bit storage however, as it can be seen in Table II, it is the -0.75V that produces the largest difference between the states of memristor.

B. Discussion

As discussed in Section III, the resistance value of memristor should show sensitivity not only to the number but also to the order of "0"s and "1"s applied to it. In other words, as shown also by simulation results, "01" and "10" inputs do no result in the same state for the memristor. The result of our simulations as shown in Table I supports the aforementioned claims and argumentation. However, as expected, the larger sensitivity is correspondent to the number of "0"s and "1"s rather than their order. Hence, even though distinct states, the resistance of "01" and "10" are closer to each other compared to the resistance of other states. The larger sensitivity to the number of "0"s and "1"s is particularly observed in Table II, in the case of "100". This case breaks the uniformity of resistance change in the table since it introduces an increase of resistance, whereas the resistance is otherwise decreasing. The reason behind this irregularity is that it entails a decrease in the number of "1"s, whereas in other transitions (from smaller to larger numbers) the number of "1"s is either equal or increasing.

Distinctiveness of various states is one of the most crucial points in using memristors as multi-bit storage. In the case of memristors as a two-bit storage unit, as seen in Table I, the difference between the critical states -namely "01" and "10"- is large enough for the majority of metering techniques to distinguish the two states. For example, in a simple basic sensing scenario, by applying a current of 0.1mA, a voltage difference of approximately 24mV between the two resistances will be observed. This voltage is two to five times larger than the smallest values that comparators such as [15], [16] can distinguish. However, the difference between the states is significantly smaller once we consider the memristors as three-bit storage units. Therefore, suitable techniques need to be explored in order to increase the distinction between different states of the memristor.

TABLE II. CHANGES OF STATES (RESISTANCE) IN A MEMRISTOR AS A 3-BIT STORAGE UNIT. PULSE WIDTH, $T = 0.1s$. MSB APPLIED FIRST.

Pattern	Negative Pulse [V]		
	-0.25	-0.5	-0.75
	Resistance of Memristor [$k\Omega$]		
"000"	6.378	7.379	8.119
"001"	5.049	6.020	6.796
"010"	4.975	5.939	6.715
"011"	3.119	3.859	4.472
"100"	4.974	5.940	6.723
"101"	3.147	3.843	4.422
"110"	3.056	3.726	4.349
"111"	0.633	0.633	0.637

Assuming that the input series is in conventional binary coding, it could be more beneficial for some applications (such as pattern learning/recognition) to modify the memristor input pulse train to supply LSB first and MSB last. This would turn the content of Table II to what we see in Table III. In this case, as we see in Table III, the states with closest values to each other are located in the vicinity of each other. In other words, the closest states (namely second and third entry as well as fifth and sixth entry of Table III) correspond to closest binary values (namely 2 and 3 as well as 5 and 6) too. In this case, if the small difference of resistance affects the output, the reading error is rather small (a mistake between 2 and 3, or 5 and 6). Whereas in case of MSB first LSB last (Table II), the small error of reading could mistake two farther located values (mistaking 2 for 4, or 3 for 5 and vice-versa).

C. Application

For memory applications, the problem of close proximity of states in a three-bit cell raises the question of whether the relatively small difference of resistance could be improved, or distinguished by reasonably sized-and-priced meters. However, for pattern learning/recognition applications the problem could be looked at from a different perspective. In other words, whether high precision and strong distinction is required or wanted. For pattern learning, it is not required to have all the bits exactly precise. Errors in few bits can be tolerated, since they will be either corrected or ignored during reconstruction of the pattern [9].

Another important aspect is the encoding and decoding of data to memristor states and vice-versa. This is an important factor, not only because of the extra load of encoding and decoding, but also because it can affect the memristor performance. As discussed before, the states are sensitive to the number and order of input bits. Binary codes are optimized for compact coding and are sub-optimal for such specific applications. Therefore, it would be beneficial to explore distinction of states by applying various digital codes. In order to take more advantage of memristor capabilities, it might be possible to develop new coding systems as well. Once the storage patterns are established, a system similar to flash Analog to Digital Converters (ADCs) [17]–[19] can be used in order to change the stored pattern back to digital. In this method two comparators with one fixed input (fixed to certain points established by the storage pattern), can determine whether the value stored is within a pre-determined range or not. The output of this flash stage can be wired to the correspondent digital output to provide proper output. In this case, usage of various digital coding casts -virtually- no extra load to the system. Therefore appropriate coding system could be adopted only internally within the memristor storage system.

For pattern recognition applications however, the process of encoding and decoding can be even simpler. In this case, one memristor stores the learned pattern and another can be used as a placeholder. The pattern under test is applied to the placeholder memristor. Then, only the analog output of the two memristors need to be compared. If the two outputs are the same, the input pattern is similar to the learned pattern and otherwise the input pattern is not recognized as known. This could unload the main processors considerably and speed up the recognition procedure significantly.

TABLE III. CHANGES OF STATES (RESISTANCE) IN A MEMRISTOR AS A 3-BIT STORAGE UNIT. PULSE WIDTH, $T = 0.1s$. LSB APPLIED FIRST.

Pattern	Negative Pulse [V]		
	-0.25	-0.5	-0.75
	Resistance of Memristor [$k\Omega$]		
"000"	6.378	7.379	8.119
"001"	4.974	5.940	6.723
"010"	4.975	5.939	6.715
"011"	3.056	3.726	4.349
"100"	5.049	6.020	6.796
"101"	3.147	3.843	4.422
"110"	3.119	3.859	4.472
"111"	0.633	0.633	0.637

V. CONCLUSION AND FUTURE WORKS

Memristor is a two terminal device with non-volatile variable resistance, with interesting characteristics. After a brief review of its construction and its behavior in Section II, we focused on the amount of change in resistance of a memristor in Section III. We showed that two similar input pulses produce two different changes, proportionate to the resistance of the memristor at each state. Afterwards, we discussed how this characteristic could be used for storing multi-bit data or patterns. We then verified this possibility via simulations, presented in Section IV. We saw that as expected, storing three bits of data proved to be more challenging than two bits. We discussed some techniques, such as coding systems other than conventional binary, that could potentially improve the performance of the system. We then pointed out that in some applications, such as patter recognition, exactness might not be as necessary as some other applications. Therefore, storing different inputs with memristor states close to each other might not lead to a substantial system error for particular applications such as pattern learning and recognition. Lastly, we briefly mentioned some interface circuits that could be potentially used for encoding and decoding data at the input and output of the memristor unit. Several avenues show promise and should be explored regarding the usage of memristors as multi-bit storage units and pattern learning agents. Specifically, we plan to examine,

- the set-up space; How internal and external parameters affect the performance and how could it be optimized?
- input characteristics; What type of input pulses (voltage and width) could improve the performance? How should they be applied to optimize the performance?
- usage of various types and models of memristor, specifically concerning practicality and implementations.
- coding space; What type of digital coding could lead to more precise and more effective storage in memristors?
- applications; What range of other applications can benefit from this characteristic of memristors and how could memristors be used?

We hope that this study will lead to a better understanding of memristors and expand their applicability across various fields

of interest. In particular, we believe that our observation could pave the way for better and more efficient learning strategies.

ACKNOWLEDGMENT

The authors would like to thank Dr. Florian Schupfer for facilitating part of the work done for this paper.

REFERENCES

[1] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on Circuit Theory,*, vol. 18, no. 5, pp. 507–519, Sep. 1971.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, 2008.

[3] L. Chua, "Resistance switching memories are memristors," *Applied Physics A*, vol. 102, no. 4, pp. 765–783, 2011.

[4] D. Biolek, M. Di Ventra, and Y. V. Pershin, "Reliable SPICE Simulations of Memristors, Memcapacitors and Meminductors," *ArXiv e-prints*, Jul. 2013.

[5] K. Eshraghian, K.-R. Cho, O. Kavehei, S.-K. Kang, D. Abbott, and S.-M. S. Kang, "Memristor MOS Content Addressable Memory MCAM: Hybrid architecture for future high performance search engines," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,*, vol. 19, no. 8, pp. 1407–1417, Aug. 2011.

[6] Y. Halawani, B. Mohammad, D. Homouz, M. Al-Qutayri, and H. Saleh, "Modeling and optimization of memristor and STT-RAM-Based memory for low-power applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,*, vol. PP, no. 99, pp. 1–1, 2015.

[7] Y. V. Pershin, S. L. Fontaine, and M. D. Ventra, "Memristive model of amoeba learning," *Physical Review E*, vol. 80, pp. 1–6, 2009.

[8] Y. Pershin and M. Di Ventra, "Neuromorphic, digital, and quantum computation with memory circuit elements," *Proceedings of the IEEE*, vol. 100, no. 6, pp. 2071–2080, Jun. 2012.

[9] J. Bian, K. Yang, E. Sidky, J. Boone, and X. Pan, "Optimization-based image reconstruction from low-dose patient breast ct data," in *IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC)*, 2013.

[10] V. Hongal, R. Kotikalapudi, and M. Choi, "Design, test, and repair of mlut (memristor look-up table) based asynchronous nanowire reconfigurable crossbar architecture," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems,*, vol. 4, no. 4, pp. 427–437, Dec. 2014.

[11] Y. Levy, J. Bruck, Y. Cassuto, E. G. Friedman, A. Kolodny, E. Yaakobi, and S. Kvatinsky, "Logic operations in memory using a memristive akers array," *Elsevier*, vol. 45, pp. 873–876, Nov. 2014.

[12] G. Gandhi, V. Aggarwal, and L. Chua, "The first radios were made using memristors!" *IEEE Circuits and Systems Magazine,*, vol. 13, no. 2, pp. 8–16, May 2013.

[13] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "Memristive switches enable stateful logic operations via material implications," *Nature*, vol. 464, pp. 873–876, 2010.

[14] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: properties of basic electrical circuits," *European Journal of Physics*, vol. 30, no. 4, p. 661, 2009.

[15] V. Katyal, R. Geiger, and D. Chen, "A new high precision low offset dynamic comparator for high resolution high speed ADCs," in *IEEE Asia Pacific Conference on Circuits and Systems 2006 (APCCAS 2006).*, Dec. 2006, pp. 5–8.

[16] J. Oliveira, J. Goes, N. Paulino, and J. Fernandes, "Improved low-power low-voltage CMOS comparator for 4-bit flash ADCs for UWB applications," in *14th International Conference on Mixed Design of Integrated Circuits and Systems, 2007 (MIXDES'07).*, Jun. 2007, pp. 293–296.

[17] C.-C. Lee, C.-M. Yang, and T.-H. Kuo, "A compact low-power flash adc using auto-zeroing with capacitor averaging," in *2013 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC),*, Jun. 2013, pp. 1–2.

[18] P. Palsodkar, P. Dakhole, and P. Palsodkar, "Improved power supply rejection (psr) digital comparator based flash analog to digital converter (fadc)," in *2014 International Conference on Electronics and Communication Systems (ICECS),*, Feb. 2014, pp. 1–5.

[19] T. Baswam, B. Harshavardhan, and E. Venkata Ramesh, "A distortion compensating flash analog-to-digital conversion using bootstrap switch," in *2014 International Conference on Advances in Electrical Engineering (ICAEE),*, Jan. 2014, pp. 1–5.