Efficient Distributed Memory Management in a Multi-Core H.264 Decoder on FPGA

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Abstract
A Distributed Shared Memory (DSM) based multi-core architecture is explored and evaluated via an H.264 decoder application. The memory access and communication over Network-on-Chips is managed by the Data Management Engine (DME).

Introduction
In this paper, a DSM based multi-core NoC architecture is explored. Each node hosts a DME connecting the core, the local memory and the network.

Demonstrator Design and Setup
The FPGA demonstrator is composed of a hardware multi-core NoC architecture and an H.264 decoder application mapping on it, while a comparing platform based on centralized memory is also presented in this section.

A. DSM Based Multi-core NoC Architecture
Fig. 1 a) shows an example of the DSM based multi-core NoC platform. As illustrated in Fig. 1 b), the local memory is partitioned into private and shared.

B. H.264 Intra Decoder
H.264 standard facilitates high compression rate and requires large amounts of computation.

C. Comparing Platforms
In order to compare with distributed memory architecture, we build a multi-core platform with a single shared memory, interconnected with an AHB bus, and also map H.264 decoder on more cores to compare the performance of distributed memory to centralized memory based platforms.

Experiment and Results
We implement above multi-core platforms on an Altera Stratix IV FPGA, running 3-node, 6-node and 9-node H.264 decoder programs to process QCIF and CIF pictures.

Conclusion
An FPGA demonstrator of a multi-core H.264 decoder supporting distributed memory has been presented.

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