Interactive Hardware-Software Partitioning and Memory Allocation Based on Data Transfer Profiling

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Abstract

This paper deals with the problems of memory allocation and partitioning in hardware/software codesign. We present two algorithms to solve these problems. First a memory allocation algorithm to minimize memory traffic is described. Second a partitioning algorithm is presented which is used to partition a C/C++ specification into behavioural VHDL and object code. The partitioning algorithm decisions are based upon information from memory allocation, execution and data transfer profiling and hardware estimations.

Summary

Every designer of complex embedded systems feels a strong need for a tool to analyse, verify and partition the system into hardware and software components in early design phases. As a result the research in codesign and related areas have accelerated enormously recently[4][7][8].

We focus our research on developing a tool for hardware/software codesign of complex embedded systems in telecommunication applications. We are developing a codesign environment called 'Akka' [1][9][10]. It takes a C/C++ specification as input to the system, this code is then compiled with several extensions to the Gnu C compiler into a database. On this database there are several programs operating and from it behavioural VHDL and object code are extracted. The hardware part is passed to the high level synthesis program SYNT[5] and then to Synopsys logic level synthesis. The hardware is implemented on a EVC[6] board, which includes a Xilinx device and fast memory on board.

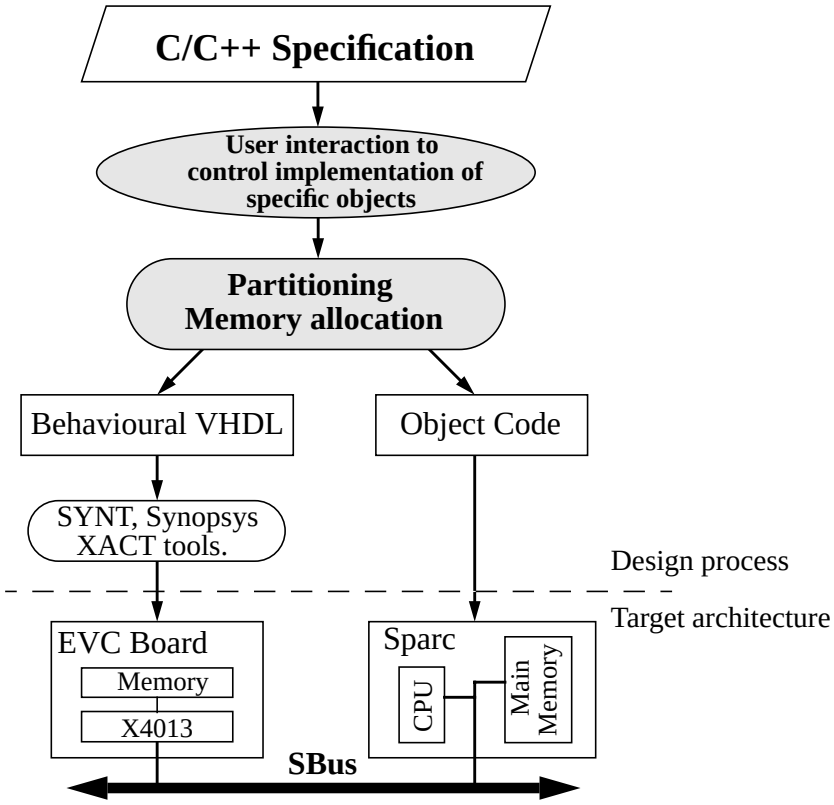

FIGURE 1. The Codesign Tool Kit, Akka.

In this paper we focus on the partitioning process and the closely related memory allocation problem. We present a memory allocation algorithm which is based on execution and data transfer profiling. Its task is to minimize the memory interface traffic and calculate a speed-up to help the partitioner to select the optimum solution. Memory allocation is one of the key issues in hardware/software partitioning since both hardware and software parts frequently have high memory requirements and communicate with each other via memory. The partitioning algorithm based on a hierarchical candidate selection scheme performs the partitioning with information from user, memory allocation, profilers and estimators. This is done efficiently by using a dynamic programming technique[3]. By respecting user directives we have made the partitioner interactive. We will show that utilizing data transfer profiling in the partitioning process can lead to significant better solutions by discussing two application examples:

A simple one, calculating the Fibonacchi numbers to illustrate the concepts, and a complex one, which models the operation and maintainance functionality in the Asynchronous Transfer Mode (ATM) protocoll [11].

The partitioning algorithm presented in this paper is based upon the work in [2] but with several improvements. In addition to its ability to handle complex data structures like classes, it considers data transfer profiling information to minimize memory traffic when allocating on board memory. This information is passed to the partitioner to get a better partitioning. The user can interactively control the partitioning phase, by deciding if an object should be implemented in software or hardware, and if the tool should generate code or use a pre-designed hardware module. He has access to all profiling and estimation data by way of an intuitive graphical user interface which allows him to get quickly a good understanding of the effects of design decisions.

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