Axel Jantsch - Complete CV

June 2013

Contents

1 Personal facts

Full name: Axel Arthur Jantsch

Born in Klagenfurt, Austria, on December 20, 1962.

Married since April 1988; 2 children.

Current position: Professor in Electronic Systems Design and Head of the Department of Electronic Systems,
School of Information and Communication Technology Royal Institute of Technology,
Electrum 229, SE-16440 Kista, Sweden

Phone: +46 8 790 4124

Fax: +46 8 752 1270

Email: axel@kth.se

Home page: web.ict.kth.se/~axel

2 Research interests

Embedded systems and dependable systems

Modeling concepts and languages

Systems on Chip architecture and design

Design methodology and tools

3 Education

1969-1973:	Volksschule St. Ruprecht, Klagenfurt, Austria.
1973-1981:	Bundesgymnasium Klagenfurt, Austria.
January 1988:	Dipl.Ing. in Informatik (Master), Vienna University of Technology, Title of thesis: *Probleme der Morphologie bei sprachanalysierenden Systemen (Morphological Problems in Language Analysis).*
December 1992:	Dr. Tech. in Computer Science (PhD), Vienna University of Technology, Title of thesis: *Design Space Exploration with Estimation Functions and Design Style Description.*
June 2000:	Docent of the Royal Institute of Technology, title of docent lecture: "Electronic Design Automation: The next 50 Years".
December 2010:	Docent at the University of Turku, Finland; Title of the docent lecture: "Predictable Communication Performance in On-Chip Networks".
Languages:	Fluent in German, English and Swedish.

4 Positions and employments

4.1 Employments

1983 - 1988:	Development of financial software and accounting systems as part time employment at Schellenberger GmbH, Vienna.
March 1988 - February 1993:	Research and teaching assistant at Institut für Technische Informatik, Technical University Vienna.
April 1993 - March 1995:	Postdoc at Electronic Systems Design Lab, Royal Institute of Technology, Stockholm, Sweden, funded by a Schrödinger grant of the Austrian Science Foundation.
June 1995 - December 1996:	Siemens Austria AG in Vienna.
Since 1996:	Royal Institute of Technology (KTH), Stockholm, Sweden; (Associate professor since 1997, full professor since 2002, head of department since 2009).

4.2 Academic positions

April 1993 - March 1995:	Postdoc at Electronic Systems Design Lab, Royal Institute of Technology, Stockholm, Sweden, financed by a Schrödinger grant of the Austrian Science Foundation.
January 1997:	Univ lektor (Associate Professor) at KTH.
June 2000:	Docent of the Royal Institute of Technology, title of docent lecture: "Electronic Design Automation: The next 50 Years".
December 2002:	Full professor in Electronic System Design at KTH.
March 2007-June 2007:	Guest Professor at Vienna University of Technology, Austria.
December 2007:	Guest Professor at Fudan University, Shanghai, China.
January 2009:	Guest Professor at University of Cantabria, Santander, Spain.
June 2009:	Guest Professor at Fudan University, Shanghai, China.
December 2010:	Docent at the University of Turku, Finland; Title of the docent lecture: "Predictable Communication Performance in On-Chip Networks".
2011-2012:	Guest professor at the Chinese Academy of Science in Shenzhen, China.

4.3 Leadership in research and education programs

January 1999 - December 2002:	Program director of the Foundation for Strategic Research (SSF) funded national research program Integrated Electronic Systems (INTELECT), with a duration of four years and a budget of 110 M SEK (1̃2 M Euro).
October 2006-June 2009:	Responsible director for the international Master Program System on Chip Design".
April 2011 - September 2012:	Coordinator of the EIT ICTLabs (www.eitictlabs.eu) Master program in Embedded Systems with participating schools: KTH, TU Eindhoven, TU Berlin, U of Trento, U of Turku, Aalto University.
Since June 2012:	Director of iPack Excellence Center, funded by Vinnova with a 3 years budget of 66 Mkr (ca. 8 M Euro) and 13 partner companies.

4.4 Industrial positions

1983 - 1988:	Development of financial software and accounting systems as part time employment at Schellenberger GmbH, Vienna.
June 1995 - December 1996:	Siemens Austria AG in Vienna.
Since September 2005:	Member of the Steering Group at FrameAccess AB.
Since September 1010:	Co-founder and Member of the Steering Group of ELSIP AB.
Since January 1012:	founder and Member of the Steering Group of Memcom.Soc Ltd.

5 Other Professional Activities

5.1 PC member

DATE (Design Automation and Test in Europe) 2001-2005, 2008-2013

FDL (Forum on Design Languages) 1998-2003

HDLCON (Hardware Description Language Conference) 2000

DCC (Designing Correct Circuits) Workshop 2004

CODES-ISSS 2003-2011, PC Co-chair in 2004, general co-chair 2005, member of the steering committee since 2006.

SoC Symposium 2003-2008

Workshop on Diagnostic Services in networks-on-Chip: TPC Co-chair in 2007 (DATE Workshop), TPC Co-chair in 2008 (DAC Workshop); Member of steering committee 2009-2011.

NoCS (International Symposium on Networks on Chip) Since 2007; member of steering committee since 2007; TPC Co-chair in San Diego 2009.

5.2 Reviewing of journal articles

IEEE Transactions of VLSI, since 1999

IEEE Transactions of Circuits and Systems, since 1999

IEEE Transactions on CAD, since 2000

Kluwer Design Automation of Embedded Systems, 2000-2002

IEEE D&T Magazine, since 2000

IEEE Computer 2002-2003

ACM Transactions on Embedded Computing Systems, since 2002

IEEE Transactions on Parallel and Distributed Systems, since 2004

IEEE Transactions on Computers, since 2006

Subject Area Editor of HW/SW Codesign for the Journal of Systems Architecture since 2002-2008

Guest editor for the special issue on Networks on Chip in the Journal of System Architecture 2003

Guest editor for the special section on Hardware/Software Codesign and System Synthesis in IEEE Transactions on VLSI Systems, Part I in August 2006 and Part II in September 2006.

Guest editor for the special issue on *C based System Level Design* of the EURASIP Journal of Embedded Systems, 2008.

Guest editor for the special issue on Networks on Chip in IEEE TCAD 2010.

5.3 Organizing conferences and workshops

Chairman of the Program Committee of the International Workshop on System Level Design Languages, Tubingen, Germany 2000.

INTELECT Workshop, Linköping, Sweden, June 1999.

INTELECT Summer Schools, ... rebro, Sweden, 2000, 2001, 2002.

EuroTraining Course on System on Chip, 3 days, Stockholm, May 2001.

Eda Träff, Stockholm, Sweden, 2000.

SSoCC 2001, 2002.

CODES-ISSS 2004 in Stockholm.

CODES+ISSS 2005 as general co-chair in New York.

Full day tutorial on Networks on Chip at DATE 2007.

Full day Workshop on Diagnostic Services in Network-on-Chips at DATE 2007.

Full day Workshop on Diagnostic Services in Network-on-Chips at DAC 2008.

iPack yearly conference in Stockholm 2012.

5.4 Project reviews

Dutch technology Foundation STW, 2003, 2004.

Academi of Finland, 2004

Engineering and Physical Science research Council, UK, 2004

King Fahd University of Petroleum and Minerals research council, 2005.

Vetenskapsråd, 2006 – NT-S committee.

Vetenskapsråd, 2008 project review.

EU FP7 Reviewer 2009, 2010, 2011, 2012

EU Artemis reviewer 2010.

EU European research Council, since 2010

5.5 Awards

Best paper nomination at the Forum on Design Languages, 1999.

Best paper award at the 10th International Conference on Field Programmable Logic and Applications, August 2000.

Best paper nomination at the Design Automation and Test in Europe Conference 2003.

Best paper nomination at the Design Automation and Test in Europe Conference 2004.

Best paper nomination at the Design Automation Conference (DAC) 2006.

5.6 Invited talks and seminars

1997

"Limitations of Interactive Design", Invited presentation at *Workshop on Electronic Design Processes*, Monterey, CA, 1997.

1998

"Formal System Specification and Refinement" at the FMV Workshop on Formal Methods in Electronics Design, Lida, Sweden, September 1998.

"System Design", EDA Gruppen regular meeting, Stockholm, December 1998.

1999

"The Rugby Model" at the Indian Institute of Technology, Delhi, India, January 1999.

"Formal System Specification Models for Verification and Refinement", EDA-Träff'99, Stockholm, Sweden, March 1999.

"Integrated Electronic Systems Program - A National Research Program", EDA-Träff'99, Stockholm, Sweden, March 1999.

"Models of Computation and Heterogeneous Simulation" at TIMA Laboratory, Grenoble, France, September 1999.

"The Rugby Model: A Frame work for the study of Modelling, Analysis and Synthesis Concepts of Electronic Systems", TU Darmstadt, November 1999.

"Models of Computation", EDA Gruppen regular meeting, Linköping, December 1999.

2000

"Integrated Electronic Systems Program", EDA-Träff 2000, Stockholm, Sweden, March 2000.

Panel member on "Challenges in SoC Education" at the IEEE NorChip Conference, Turku, Finland, November 2000.

"The Integrated Electronics Systems Research Program", SSF Program Conference, Stockholm, November 2000.

2001

Axel Jantsch, System Modelling - Models of Computation and their Applications, Presentation at System-on-Chip Design at the Graz University of Technology (50 min), April 2001.

Axel Jantsch, International Master of Science Program in System-on-Chip Design at KTH, Presentation at System-on-Chip Design at the Graz University of Technology (10 min), April 2001.

Axel Jantsch, The Usage of Stochastic Processes in Embedded System Specifications, Presentation at the HW/SW Codesign Symposium in Copenhagen (20 min), April 2001.

Axel Jantsch, System Modelling - Models of Concurrency and their Applications (4h), Presentation at Jönköping University, April 2001.

Axel Jantsch, Introduction to Haskell and ForSyDe, Presentation at KTH (1h), March 2001.

Axel Jantsch, HW/SW Codesign (4h), Presentation at Jönköping University, May 2001.

Axel Jantsch, System Modelling and SDL-Matlab Cosimulation (2h), Presentation at the Eurotraining System-on-Chip Course, May 2001.

Axel Jantsch, Industrial Ph.D. Projects (30min), Presentation at the Industrial Research Seminar at SaabTech, Stockholm, Sweden, September 2001.

Axel Jantsch, Introduction to Networks on Chip (30min), Workshop at the European Solid-State Circuit Conference (ESSCIRC), Villach, Austria, September 2001.

Axel Jantsch, Network-on-Chip Architectures (30min), Workshop at the European Solid-State Circuit Conference (ESSCIRC), Villach, Austria, September 2001.

Axel Jantsch, Models of Computation in Embedded System Design (50 min), Presentation at the Department of Computer Science at Linköping University, September 2001.

Axel Jantsch, Embedded Software/System in the SOC Master Program, Presentation at the Socware Education workshop, November 2001.

2002

Axel Jantsch, A Template for Distance Learning Courses without Loss of Quality, Presentation at the SoC SME Workshop, April 2002.

Axel Jantsch, Networks on Chip, Presentation at the Conference RadioVetenskap och Kommunikation, June 2002.

Axel Jantsch, Networks on Chip: A Paradigm Change?, Presentation at the SOCWare Day, Kista, November 2002.

Axel Jantsch, Network on Chip Architecture, Presentation at the EXCITE Workshop, Helsinki, November 2002.

Axel Jantsch, Networks on Chip, Presentation at the SoC Architecture Course at KTH, December 2002.

2003

Networks on chip - status of Nostrum. Invited Presentation at Darmstadt University of Technology, April 2003.

What is a good platform? Presentation at the EDA Gruppen Meeting, February 2003.

Communication Refinement for a Network-on-Chip Platform, Invited presentation at MPSOC'03 - International Seminar on Application- Specific Multi-Processor SoC, Chamonix, France, July 2003.

Networks on Chip, Invited keynote at DSD'2003 - Euromicro Symposium on Digital System Design, September 2003.

System Specification Fundamentals, Invited presentation at the Medea+ DAC Conference, Stuttgart, November 2003.

Network on Chip Tutorial. Invited lecture at the Stringent Summer School, August 2003, Örebro, Sweden.

Networks on Chip. Invited tutorial at the IEEE NorCHIP Conference, Riga, Latvia, November 2003.

The Nostrum network on chip. Invited presentation at ProRISC, Eindhoven, November 2003.

2004

The Nostrum network on chip. Guest lecture in the SoC Architecxture course, KTH, December 2004.

Networks on chip. Invited seminar at Linköping University, November 2004.

2005

The Nostrum network on chip. Invited Seminar at Åbo Akademi, Turku, Finland, March 2005.

Axel Jantsch, Robert Lauter, and Arseni Vitkowski. *Power analysis of link level and end-to-end protection in networks on chip.* Invited presentation for the special session on Networks on Chip at ISCAS, May 2005.

The Nostrum network on chip. Invited presentation at the International Symposium on System-on-Chip, Tampere, Finland, November 2005.

The Nostrum network on chip. Invited presentation at Lancaster University, October 2005.

NoC: A new contract between hardware and software? Invited seminar at Lancaster University, October 2005.

2006

Compositional traffic in networks on chip. Invited presentation at the Baltic Electronic Conference, October 2006.

Communication performance in network-on-chips. Short course at Tallinn Technical University, October 2006.

Exchange of course modules across universities. Invited presentation at the 6th European Workshop on Microelectronic Education, June 2006.

Models of computation for networks on chip. Invited talk at the Sixth International Conference on Application of Concurrency to System Design, June 2006 Standards for NoC: What can we gain? Invited presentation at the DATE Workshop on Future Interconnect and NoC, March 2006.

Tiberius Seceleanu, Axel Jantsch, and Hannu Tenhunen. On-chip distributed architectures. Tutorial at the International SoC Conference, September 2006. Austin, Texas.

Axel Jantsch, ForSyDe: A Denotational Framework for Heterogeneous Models of Computation, Invited Presentation at the ARTIST workshop Models of Computation and Communication, November 2006.

2007

Axel Jantsch. NoC: State of the art, trends and challenges. Section I of Full Day Tutorial *NoC at the Age of Six: Advanced Topics, Current Challenges and Trends* given by Axel Jantsch, Luca Benini, Timothy M. Pinkston, Kees Goossens, Pieter van der Wolf, Alian Fanet and Marcello Coppola at DATE 2007, April 2007

Axel Jantsch. Performance analysis and dimensioning of bandwidth and buffer capacity. Section I of Full Day Tutorial on *Networks on Chip* given by Axel Jantsch, Luca Benini and Radu Marculescu at the NoC Symposium 2007, May 2007

Axel Jantsch, Models of Computation for Networks on Chip, Invited Seminar at IMEC, February 2007.

Axel Jantsch and Zhonghai Lu, Slot allocation using logical networks for TDM virtual circuit configuration for network-on-chip, Invited Seminar at Eindhoven University of Technology, November 2007.

Axel Jantsch, The Nostrum Network on Chip, Invited Seminar at Turku Center for Computer Science, November 2007.

Axel Jantsch, *Network Layer Communication Performance in Network-on-Chips*, Section I of a half day tutorial "Tutorial on Networks on Chip" at the ASP-DAC 2008, January 2007.

2008

Axel Jantsch. Network layer communication performance in networks on chip. Tutorial at the Asian Pacitific Design Automation Conference given by Axel Jantsch and Dave Gwilt, January 2008

Axel Jantsch. A formal framework for heterogeneous models of computation. Tutorial on *Heterogeneous System Level Specification using SystemC* given by Eugenio Villar, Axel Jantsch, Christoph Grimm and Tim Kogel at Design Automation and Test Conference (DATE), March 2008

Axel Jantsch, Nostrum Network on Chip, Invited Seminar at the Turku center of Computer Science, April 2008.

Axel Jantsch and Zhonghai Lu, Quality of Service in Networks on Chip, Invited Seminar at the Research Center Telecommunciation Vienna (FTW), April 2008.

Axel Jantsch. Nostrum network on chip. Invited Seminar at the Turku center of Computer Science, April 2008.

2009

Axel Jantsch and Zhonghai Lu. Trends in terascale on-chip computing 2010-2020. Invited Seminar at the ICES annual conference, September 2009.

Axel Jantsch and Zhonghai Lu. Trends in terascale on-chip computing 2010-2020. Invited Seminar at Nanjing University, July 2009.

Axel Jantsch et al. The Nostrum network on chip. Invited Seminar at Fudan University, June 2009.

Axel Jantsch and Zhonghai Lu. Networks on chip. Short course at Fudan University, June 2009.

Axel Jantsch. Resource allocation for quality of service on-chip communication. Invited seminar at the University of Cantabria, Santander, Spain, February 2009.

Axel Jantsch. Resource allocation for quality of service on-chip communication. Invited seminar at the real Time Research Center in Vasteras, Sweden, February 2009.

Axel Jantsch et al. The Nostrum network on chip. Invited Seminar at Fudan University, June 2009.

Axel Jantsch and Zhonghai Lu. Trends in terascale on-chip computing 2010-2020. Invited Seminar at Nanjing University, July 2009.

Axel Jantsch and Zhonghai Lu. Trends in terascale on-chip computing 2010-2020. Invited Seminar at the ICES annual conference, September 2009.

2010

Axel Jantsch, Matthew Grange, and Dinesh Pamunuwa. Promises and limitations of 3-D integration. Seminar at NUDT, Changsha, China, December 2010.

Axel Jantsch, Xiaowen Chen, Abdul Naeem, Yuang Zhang, Sandro Penolazzi, and Zhonghai Lu. Memory architecture and management in a NoC platform. Seminar at Fudan University, Shanghai, China, December 2010.

Axel Jantsch. Network on chip. Seminar at the Huawei-Fudan Workshop, Shanghai, China, December 2010.

Axel Jantsch, Xiaowen Chen, Abdul Naeem, Yuang Zhang, Sandro Penolazzi, and Zhonghai Lu. Memory architecture and management in a NoC platform. Seminar at Nanjing University, Nanjing, China, December 2010.

Axel Jantsch. Predictable communication performance in on-chip networks. Docent Lecture at University of Turku, Finland, December 2010.

2011

Axel Jantsch, Xiaowen Chen, Zhonghai Lu, Chaochao Fao, Abdul Nameed, Yang Zhang, and Ahmed Hemani. Memory architecture and management in a NoC platform. Tutorial at Design Automation and Test Conference (DATE), March 2011.

Axel Jantsch. Predictable communication performance in on-chip networks. Invited Seminar at University of Technology Vienna, June 2011

Axel Jantsch. Shared memories in multiprocessors. Lecture at the Shenzhen Summer School on Embedded Systems, July 2011

Axel Jantsch. ForSyDe: A formal framework for heterogeneous models of computation. Invited Seminar at the Shenzhen Institute of Advanced Technology, Chinese Acadamy of Science, September 2011

Axel Jantsch. ForSyDe: A formal framework for heterogeneous models of computation. Invited tutorial at the International Symposium on Systems on Chip, November 2011

Axel Jantsch. Computational limits in 3-d integrated systems. Keynote at the International Symposium on Systems on Chip, November 2011

2012

Martin Radetzki, Xueqian Zhao, Chaochao Feng, and Axel Jantsch. Fault tolerance in networks on chip. Tutorial at the Network on Chip Symposium 2012,

May 2012

Axel Jantsch. Memory architectures in heterogeneous multicore SoCs. European Nanoelectronics Design Technology Conference, June 2012

Axel Jantsch, Marco Bekooij, Alan Burns, Abbas E. Kiasari, and Zhonghai Lu. Analytical approaches for performance evaluation of networks on chip. ESWeek Tutorial, October 2012

2013

Axel Jantsch, Awet Yemane Weldezion, Dinesh Pamunuwa, and Matt Grange. The zero-load predictive model for 3d nocs. Invited talk at the Design for 3D Silicon Integration Workshop, June 2013

6 Main research contributions

Development of a HW/SW codesign system, named Akka, as a post doctoral scholar at KTH, 1993-1995. The main contributions were a partitioning algorithm based on dynamic programming, a cosimulation environment, a coemulation environment, a profiling method for performance estimation, and a graphical front-end to visualize design properties. This activity eventually led to 1 Licentiate thesis, 1 PhD thesis, a few Master theses, and initiated the HW/SW codesign activity at the Royal Institute of Technology.

Development of a **formal framework for models of computation** that is based on deterministic process networks. Based on the concepts described in *Modeling Embedded Systems and SoCs - Concurrency and Time in Models of Computation*, Morgan Kaufmann Publishers, June 2003, the ForSyDe modelling and design methodology has been developed together with Ph.D. students Ingo Sander, Wenbiao Wu, Tarvo Raudvere, Ashish Singh, Zhonghai Lu, Jun Zhu at the Royal Institute of Technology. Since then Ingo Sander has become Associate Professor and is now leadiong this research activity.

Development of **Nostrum**, the KTH Network on Chip together with Ahmed Hemani, Shashi Kumar, Zhonghai Lu, Mikael Millberg, Erland Nilsson, Richard Thid, Johnny Öberg and others. Nostrum is based on a buffer-less, loss-less minimal switch architecture that offers both best effort and guaranteed bandwidth services. Starting in the year 2000 this activity was among the first and pioneering research in the NoC field.

Development of **McNoC**, an on-chip distributed shared memory architecture based on our Nostrum NoC. Based on the observation that the memory access bottleneck is becoming more and more severe, and on the prospect that 3D integration will allow the integration of massive amounts of DRAM into a stacked system with very high memory bandwidth for each individual core, we started to develop a DSM (Distributed Shared Memory) architecture. At the

centre of this architecture is a programmable controller, called the DME (Data Management Engine), that can realize virtual-to-physical address translation, cache coherence protocols, memory consistency models and dynamic memory allocation algorithms in microcode. So far this work has resulted in a number of publications, a patent submission and industrial collaboration with ST Microelectronics in Grenoble and Huawei in Sweden and Shanghai, and in 2 spin-off companies (ELSIP in 2010, Memcom in 2012).

Development of a **compositional performance analysis method** for SoCs and embedded systems. This method is based on Network Calculus and allows for worst case timing analysis, dimensioning of platform resources and for traffic shaping. This method is also applied in wireless sensor networks. In 2011 this activity has resulted in a cooperation project with Intel. My former Ph.D. student has become Associate Professor and is now leading this effort.

7 Experience in management

Deputy Head of Laboratory (Biträdande avdeliningschef) at the Electronics System Design Laboratory (ESDlab), Department for Electronics (ELE), KTH, May - December 1998.

January 1999-December 2002 I was general manager of SSF's (Stiftelsen för strategisk forskning) program *Integrated Electronic System*s, which involves groups from four Universities (KTH, LiTH, LTH, CTH) and has a four year budget of 110 MSEK (€13 M).

January 2004-September 2005 I was head the Laboratory for Electronics and Computer Systems (LECS), which hosted 8 professors and in total 65 persons. As head I had financial and personell responsibility.

Since July 2009 I am head of the Electronic Systems Department with 60 persons and a yearly budget of 40 MSEK (€4.7 M).

Since June 2012 I am director of the iPack excellence center, which is ten years research program funded by Vinnova with a yearly budget of 22 MSEK (€2.6 M).

8 Grants and research contracts

Project name	Period	Funding Agency	Amount	Note
Schrödinger Scholarship	1993-1995	Austrian Science Foundation	ÖS 600 k	
AASIC Consortium	1997-1999	SSF (Strategic Research Foundation)	SEK 2.5 M	Industrial participation
SAVE	1998-2000	NUTEK	SEK 1.3 M	50% industrial cofunding
MASCOT	1998-2002	SaabTech	SEK 600 k	+ fulltime Ph.D. student
ArchDes	1999-2000	Jönköping School of Engineering	SEK 400 k	+ fulltime Ph.D. student
Protocol Processor	1999-2002	SSF/Intelect	SEK 2.4 M	Industrial participation
MASIC	1999-2002	SSF/Intelect	SEK 1.8 M	Industrial participation
Low Power Operating Systems	2000-2003	SSF/Intelect	SEK 1.8 M	Industrial participation
System Specification and Verification	2001-2003	SSF/Intelect	SEK 1.2 M	Industrial participation
Formal System Design	1999-2003	SSF/Intelect	SEK 1.6 M	Industrial participation
NOCARC	2001-2003	Vinnova	SEK 3 M	50% industrial cofunding
NOC Design Methodology	2001-2004	SOCWare	SEK 2.25 M	Industrial participation
NOC Evaluation	2002-2005	SOCWare	SEK 1.5 M	Industrial participation
SOC-SME	2002-2004	Nordisk Industri Fond	NOK 900 k	50% cofunding
SOC-Mobinet	2002-2004	EU	€ 870 k	50% industrial cofunding;Main applicant: H. Tenhunen
SaverNOC	2005-2007	SaabTech	SEK 360 k	+ fulltime Ph.D. student
SPRINT	2006-2008	EU	€ 304 k	IP project, Philips Semiconductor is coordinator
ANDRES	2006-2008	EU	€ 223 k	STREP project, OFFIS is coordinator
HET-MoC	2006-2008	Swedish Research Council	SEK 2.2 M	
MOSART	2008-2011	EU	€ 247 k	STREP project, Thales is coordinator
SYSMODEL	2009-2011	EU Artemis	€ 360 k	
NoC ADM	2009-2011	Swedish Resarch Council	SEK 2.4 M	
NoC Evaluation	2010-2011	Huawei Sweden AB	SEK 1.5 M	
iFEST	2010-2013	EU Artemis	€ 300 k	ABB is coordinator
DME Verification	2010-2013	Vinnova	SEK 2 M	Research commercialization project
NoC Performance Analysis	2011-2013	Intel Inc in USA	US$ 300 k	
iPack Excellence Center	2013-2016	Vinnova	SEK 66 M	10 year center; decision taken for 3 years; 13 companies with cofunding;

9 Experience in Undergraduate Education

9.1 Course responsible

Silicon Compilation, 5th year, TU Vienna, Austria, 1990, 1991, 1992

Concurrent Engineering, 4th year, Royal Institute of Technology, 1995, 1996, 1997, 1998, 1999, 2000.

Advanced Topics in System Synthesis, Graduate Course, Royal Institute of Technology, 1999-2003, 2006, 2009, 2010.

System Modelling, 4th year, Royal Institute of Technology, 2001, 2002, 2003, 2004, 2005, 2006, 2007, 2008. This course was given for the E section students, for the IT-University students and for the Master program in System-on-Chip.

Advanced Topics in System Modelling, Graduate Course, KTH, 2001-2012.

Embedded Systems, 4th year, Royal Institute of Technology, 2001, 2002; This course is given for the E section students, for the IT-University students and for the Master program in System-on-Chip students.

System Modelling. A SoC-Mobinet course given at Denmark Technical University, Lyngby, Denmark, February-May 2004.

System Modeling. A distance learning course offered to small and medium enterprises in the five nordic and three Baltic countries as part of the SoC-SME project, January-September 2004.

System Modeling. Guest lecturer at University of Technology Vienna, Austria, March 2007 – June 2007.

System on Chip Architecture. Full course given in December 2007 – January 2008 at Fudan University, Shanghai, China.

SoC Design Project Course for SoC Design students; 2007 - 2010.

SoC Architecture at KTH; 2008 - 2012.

Embedded Systems Design at KTH in 2013.

9.2 Master thesis supervision

I have supervised or examined 110 masters theses in the years 1992-2013.

9.3 Invited course lectures

NorESD Seminar Series, lectures on *HW/SW Cosimulation*, Stockholm, Sweden, April 1993.

NorESD Seminar series, lectures on *HW/SW Codesign and Performance Estimation*, Stockholm, Sweden, April 1994.

HW/SW Codesign, Graduate Course, Linköping University, Sweden, 1998, lecture on *Concurrent Engineering*.

Embedded Systems course, 4^{th} year, in Jönköping University, Sweden, February 2000, lecture series on S*ystem Methodologies.*

Embedded Systems course, 4^{th} year, in Jönköping University, Sweden, March 2000, lecture series on *System Modelling and Specification.*

Datorsystem, 4th year, in Midhögskolan Sundsvall, Sweden, April 2000, lecture on *System Modelling and Specification.*

System on Chip Eurotraining Course, Grenoble, France, May 2000, lecture on *Models of Computation.*

System on Chip Eurotraining Course, Lyngby, Denmark, November 2000, lecture on *Models of Computation.*

System on Chip Eurotraining Course, Stockholm, Sweden, May 2001, lecture on *Models of Computation.*

Embedded Systems Course in SOC Master Program, Royal Institute of Technology, Stockholm, Sweden, October 2000, lectures on *Microprocessor Architectures, Compiler Techniques, Hardware Acceleration, Networks.*

9.4 Publications and presentations on education

L. Hellberg, A. Hemani, J. Isoaho, A. Jantsch, M. Mokhtari, and H. Tenhunen. System oriented vlsi curriculum at kth. In *Proceedings of the International Conference on Microelectronic Systems Educations, MSE97*, 1997

L. Hellberg, A. Hemani, J. Isoaho, A. Jantsch, M. Mokhtari, and H. Tenhunen. Integration of physical and functional electronic system representations in electronic curriculum. In *Proceedings of the 15th NORCHIP Conference*, 1997

Tero Nurmi, Hannu Tenhunen, Li-Rong Zheng, Axel Jantsch, Jari Nurmi, and Jouni Isoaho. Physical performance modelling for platform-based SoC design. In *Proceedings of the 4th European Workshop on Microelectronics Education*, May 2002

Ingo Sander, Axel Jantsch, and Hannu Tenhunen. The platform as interface in a SoC design curriculum. In *Proceedings of te 5t European Worksop on Microelectronics Education*, April 2004

System-on-chip education. Panel Presentation at NorChip 2000, Turku, Finland, November 2000.

International master of science program in system-on-chip design at KTH. Presentation at System-on-Chip Design at the Graz University of Technology, Graz, Austria, April 2001.

Industrial Ph.D. projects. Presentation at the Industrial Research Seminar at SaabTech, Stockholm, Sweden, September 2001.

Embedded software/system in the SOC Master program. Presentation at the Socware Education workshop, November 2001.

Exchange of Course Modules across Universities, Invited presentation at the 6th European Workshop on Microelectronic Education, June 2006.

9.5 Other activities in education

In autumn 1998 I was consultant in the definition process for the fourth year of the master program *Embedded Systems* at the Jönköping Ingenjörshögskolan. In 1999 a master of science education in *Embedded Systems* has been established for the first time at the Ingenjörshögskolan in Jönköping. Therefore, a fourth year had to be defined on top of the three year education programs already in place. I was thoroughly involved in this process and much of the current curriculum structure and many courses are based on my proposal.

In 2000 I contributed to the definition of the Royal Institute of Technology's IT-University curriculum in the circuits and systems line.

In 2000 I contributed to the definition of the Royal Institute of Technology's Master Program in System-on-Chip, which has been further developed since then with my active participation and contribution.

October 2006 – June 2009 I was responsible director for the International Master Program "System on Chip Design".

Since March 2009 I have participated in the steering group for defining a new International master Program on Embedded Systems at KTH. The program has been approved and will start operation in the fall 2011.

From fall 2010 to fall 2012 I was coordinator of the consortium applying for an EIT ICT Master School (http://eit.ictlabs.eu/) in Embedded Systems. Consortium members are KTH, Alto University in Helsinki, TU Berlin, 3TU in the Netherlands, TUCS in Finland, University of Trento in Italy. The program has started in 2011 and I have coordinated it during the start-up period.

10 Experience in Postgraduate Education

10.1 Ph.D. Thesis supervision

1. Mattias O'Nils. *Specification, Syntheisis and Validation of Hardware/Software Interfaces*. PhD thesis, Department of Electronics, Royal Institute of Technology, Stockholm, Sweden, June 1999
2. Per Bjuréus. *High-Level Modeling and Evaluation of Embedded Real-Time Systems*. PhD thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, Stockholm, Sweden, June 2002. TRITA-IMIT-LECS-02-03
3. Ingo Sander. *System Modeling and Design Refinement in ForSyDe*. PhD thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, Stockholm, Sweden, May 2003. TRITA-IMIT-LECS AVH 03:03
4. Abhijit Kumar Deb. *System Design for DSP Applications with the MASIC Methodology*. PhD thesis, Royal Institute of Technology, Stockholm, September 2004
5. Tarvo Raudvere. Verification of local design refinements in a stystem design methodology. Licentiate thesis, Royal Institute of Technology, Stockholm, April 2004
6. Tarvo Raudvere. *System Level Techniques for Verification and Synchronization after Local Design Refinements*. PhD thesis, Royal Institute of Technology, Stockholm, August 2007. ISBN 978-91-7178-677-7, TRITA-ICT/ECS AVH 07:05
7. Zhonghai Lu. Using wormhole switching for networks on chip: Feasibility analysis and microarchitecture adaptation. Licentiate thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, June 2005
8. Zhonghai Lu. *Design and Analysis of On-Chip Communication for Network-on-Chip Platforms*. PhD thesis, Royal Institute of Technology, Stockholm, March 2007. ISBN 978-91-7178-580-0, TRITA-ICT/ECS AVH 07:02
9. Iyad Al-Khatib. *Performance Analysis of Application Specific Multicore Systems on Chip*. PhD thesis, School of Information and Communication Technology, Royal Institute of Technology, Isafjordsgatan 39, 16440 Kistam, Sweden, June 2008. TRITA-ICT/ECS AVH 08:06
10. Ming Liu. A high-end reconfigurable computation platform for particle physics experiments. Licentiate thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, November 2008

11. Ming Liu. *Adaptive Computing based on FPGA Run-Time Reconfigurability.* PhD thesis, Royal Institute of Technology, Isafjordsgatan 39, SE-16440 Kista, Sweden, June 2011. TRITA-ICT/ECS AVH 11:05

12. Jun Zhu. Energy and design cost efficiency for streaming applications on systems-on-chip. Licentiate thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, May 2009

13. Jun Zhu. *Performance Analysis and Implementation of Predictable Streaming Applications on Multiprocessor Systems-on-Chip.* PhD thesis, Royal Institute of Technology, Isafjordsgatan 39, SE-16440 Kista, Sweden, December 2010. TRITA-ICT/ECS AVH 09:02

14. Huimin She. Network-calculus-based performance analysis for wireless sensor networks. Licentiate thesis, School for Information and Communication Technology, Royal Institute of Technology, Stockholm, Sweden, June 2009

15. Mikael Millberg. *Architectural Techniques for Improving Performance in Networks on Chip.* PhD thesis, Royal Institute of Technology, Isafjordsgatan 39, SE-16440 Kista, Sweden, December 2011

16. Huimin She. *Performance Analysis and Deployment Techniques for Wireless Sensor Networks.* PhD thesis, School of Information and Communication Technology, Royal Institute of Technology, Isafjordsgatan 39, 16440 Kistam, Sweden, May 2012. TRITA-ICT/ECS AVH 12:02

17. Abdul Naeem. *Architecture Support and Scalability Analysis of Memory Consistency Models in Network-on-Chip based Systems.* PhD thesis, School of Information and Communication Technology, Royal Institute of Technology, Isafjordsgatan 39, 16440 Kistam, Sweden, February 2013. TRITA-ICT/ECS AVH 12:11

10.2 Thesis evaluation

Opponent in Licentiate defenses:

Erik Stoy, *A Petri Net Based Unified Representation for Hardware/Software Co-Design*, Licentiate thesis, Linköping University, 1995.

Tomas Henriksson, *Hardware Architecture for Protocol Processing*, Institute of Technology, Linköping University, Linköping, Sweden, Licentiate thesis, December 2002.

Luis Alejandro Cortes, *A Petri Net based Modeling and Verification Techniques for Real-Time Embedded Systems*, Institute of Technology, Linköping University, Linköping, Sweden, Licentiate thesis, December 2002.

Filip Sebek, *Instruction Cache Memory Issues in real-time Systems,*Department of Computer Science and Engineering, Mälardalen University, VästerŒs, Sweden, Licentiate thesis, September 2002.

Per Andersson, *Modelling and Implementation of a Vision System for Embedded Systems*, Licentiate thesis, Department of Computer Science, Lund University, Lund, Sweden, LU-CS-LIC:2003-1, January 2003.

Benny Thörnberg, *Memory Modeling and Synthesis for Real-time Video Processing Systems*, Mid Sweden University, 2004.

Rickard Holsmark, Deadlock Free Routing in Mesh networks on Chip with Regions, Linköping University, SE-58183 Linköping, Sweden, Licentiate thesis, 2009.

Opponent and expert evaluator for Ph.D. theses:

Juha Plosila, *Self-Timed Circuit Design - The Action System Approach*, University of Turku, Turku, Finland, June 1999.

Tiberiu Seceleanu, *Systematic Design of Synchronous Digital Circuits*, PhD thesis, Turku Centre for Computer Science, Turku, Finland, TUCS Dissertations No 32, May 2001.

Dag Björklund, *A Kernel Language for Unified Code Synthesis*, Turku Center for Computer Science, February 2005.

Basant Kumar Dwivedi, *Synthesizing Application Specific Multiprocessors Architectures for Process Networks*, IIT Delhi, New Delhi, India, 2005.

David Sigüenza Tortosa, Proteo: *The Development of a Practical Network-on-Chip*, Tampere University of Technology, Tampere, Turku, 2005.

Heikki Kariniemi, ON-LINE RECONFIGURABLE EXTENDED GENERALIZED FAT TREE NETWORK-ON-CHIP FOR MULTIPROCESSOR SYSTEM-ON-CHIP CIRCUITS, Tampere University of Technology, Tampere, Finland 2006.

Xin Wang, *Designing Globally-Asynchronous Locally-Synchronous On-Chip Communication Networks*, Tampere University of Technology, Tampere Finland 2008.

Zheng Shi, Real-time Communication Services for Networks on Chip, PhD thesis, Department of Computer Science, University of York, York. Y010 5DD, UK, February 2010.

Thorsten Mähne, Efficient Modelling and Simulation Methodology for the Design of Mixed-Signal Systems on Chip, PhD thesis, ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE, February 2011.

Member of evaluation committee for Ph.D. theses:

Ingemar Söderquist, *CMOS Circuits for Digital Systems*, PhD thesis, Department of Electrical Engineering, Linköping University, Dissertation No. 775, October 2002.

Paul Popp, *Analysis and Synthesis of Communication Intensive Heterogeneous Real-Time Systems*, PhD thesis, Institute of Technology, Linköping University, Dissertation No. 833, June 2003.

Daniel Eckbert, *Power Estimation and Multi-Phase Clock Generation for the Deep Submicron Era*, Department of Computer Engineering School of Computer Science and Engineering, Chalmers University of Technology, Göteborg, Sweden, December 2003

Joe Armstrong, *Making reliable distributed systems in the presence of software errors*, PhD thesis, Department of Microelectronics and Information Technology, Royal Institute of Technology, November 2003.

Ulf Nordqvist, Protocol Processing in Network Terminals, Linköping University, 2004.

Luis Cortes, Verification and Scheduling Techniques for Real-time Embedded Systems, Linköping University, Sweden, 2005.

Paul Pop, *Analysis and Synthesis of Communication-Intensive Heterogeneous Real-Time Systems*, Ph. D. Thesis No. 833, Dept. of Computer and Information Science, Linköping University, June 2003

Sorin Manolache, Analysis and Optimisation of Real-Time Systems with Stochastic Behaviour, Linköping University, Linköping, Sweden 2005.

Benny Thörnberg, Memory Modeling and Synthesis for Real-Time Video Processing Systems, Mid-Sweden University, Sundsvall, Sweden 2006.

Antonis Papanikolaou, *Application-driven Software Configuration of Communication Networks and Memory Organizations*, Gent University, Belgium 2006.

Sander Stuijk, *Predictable Mapping of Streaming Applications on Multiprocessors*, Technical University Eindhoven, The Netherlands, November 2007.

Martin Holzer, *Design Space Exploration for the Development of Embedded Systems*, Vienna University of Technology, Vienna, Austria 2008.

Ari Kulmala, Scalable Multiprocessor System-on-Chip Architecture Design on FPGA, PhD thesis, Tampere University of Technology, Tampere, Finland, 2008.

Najeem Lawal, Memory Synthesis for FPGA Implementation of Real-Time Video Processing Systems, PhD thesis, Mid Sweden University, Sundsvall, Sweden, ISBN 978-91-86073-26-8, January 2009.

Wang Xin, Designing Globally-Asynchronous Locally-Synchronous On-Chip Communication Networks, PhD thesis, Tampere University of Technology, Tampere, Finland, 2008.

Fernando Herrera Casanueva, Heterogeneous Specification and Automatic Software Generation from SystemC for Embedded Systems, PhD thesis, University of Cantabria, Santander, Spain, January 2009.

Matthias Bo Stuart, Modelling, Synthesis and Configuration of Networks-on-Chip, PhD thesis, Technical University Denmark, May 2010.

Markus Winter, Unterstützung und Organisation von Quality-of-Service Techniken in Kommunikationsnetzwerken auf einem Chip, PhD thesis, Technical University Dresden, December 2011.

Abdoulaye Gamatie, Design and Analysis for Multi-Clock and Data-intensive Applications on Multiprocessor Systems-on-Chip, Habilitation thesis, LIFL Labratoire d'Informatique Fondamenatale de Lille, France, November 2012.

Freek Verbeek, Formal Verification of on-chip communication fabrics, Ph.D. thesis, Radboud University Nijmegen, The Netherlands, March 2013.

Imram Mahmood, A Verification Framework for Component Based Modeling and Simulation, Ph.D. thesis, Royal Institute of Technology, February 2013.

Magnus Persson, A Formalized Approach to Multi-View Components for Embedded Systems, Ph.D. thesis, Royal Institute of Technology, June 2013.

11 Peer reviewed publications

Between 1992 and 2013 I have published over 250 peer reviewed contributions:

197 papers in international conferences

40 journal articles

15 book chapters

5 books as editor

1 book as author

Citations on Google Scholar:

http://scholar.google.se/citations?user=ZF4gC44AAAAJ&hl=sv

Axel Jantsch

Google scholar

Royal Institute of Technology - KTH
Unknown interests
Verified email at kth.se

Citation indices

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h-index	27	25
i10-index	90	56

Citations to my articles

Show: 20 **1-20** Next >

Title / Author	Cited by	Year
A network on chip architecture and design methodology S Kumar, A Jantsch, JP Soininen, M Forsell, M Millberg, J Oberg, K Tiensyrja ... VLSI, 2002. Proceedings. IEEE Computer Society Annual Symposium on, 105-112	1006	2002
Will networks on chip close the productivity gap? A Jantsch, H Tenhunen Networks on chip, 3-18	627	2004
Network on chip: An architecture for billion transistor era A Hemani, A Jantsch, S Kumar, A Postula, J Oberg, M Millberg, D Lindqvist Proceeding of the IEEE NorChip Conference, 166-173	360	2000
Guaranteed bandwidth using looped containers in temporally disjoint networks within the Nostrum network on chip M Millberg, E Nilsson, R Thid, A Jantsch Design, Automation and Test in Europe Conference and Exhibition, 2004 ...	316	2004
Modeling embedded systems and SoCs: concurrency and time in models of computation A Jantsch Morgan Kaufmann Pub	204	2004

Books

[1] Axel Jantsch and Hannu Tenhunen, editors. *Networks on Chip*. Kluwer Academic Publishers, February 2003.

[2] Axel Jantsch. *Modeling Embedded Systems and SoCs - Concurrency and Time in Models of Computation*. Systems on Silicon. Morgan Kaufmann Publishers, June 2003.

[3] Axel Jantsch, Johnny Öberg, and Hannu Tenhunen, editors. *Journal of Systems Architecture*, volume 50. Elseviere, February 2004. Special Issue on Networks on Chip.

[4] Jari Nurmi, Hannu Tenhunen, Jouni Isoaho, and Axel Jantsch, editors. *Interconnect-Centri Design for Advanced SoCs and NoCs*. Kluwer Academic Publisher, April 2004.

[5] Axel Jantsch and Dimitrios Soudris, editors. *Scalable Multi-core Architectures: Design, Methodologies, and Tools*. Springer, 2011.

[6] Abbas Sheibanyrad, Frédéric Pétrot, and Axel Jantsch, editors. *3D Integartion for NoC-based SoC Architectures*. Integrated Circuits and Systems. Springer, January 2011.

Journal Articles

[1] Axel Jantsch, Shashi Kumar, and Ahmed Hemani. A metamodel for studying concepts in electronic system design. *IEEE Design & Test of Computers*, 17(3):78–85, July-September 2000.

[2] Axel Jantsch, Johann Notbauer, and Thomas Albrecht. Functional validation for large telecom systems. *Design Automation of Embedded Systems, Kluwer*, 5(1), February 2000.

[3] Per Bjuréus and Axel Jantsch. Modeling of mixed control and dataflow systems in MASCOT. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 9(5):690–704, October 2001.

[4] Johnny Öberg, Mattias O'Nils, Axel Jantsch, Adam Postula, and Ahmed Hemani. Grammar-based design. *Journal of Systems Architecture*, 47(3-4):225–240, April 2001.

[5] Mattias O'Nils and Axel Jantsch. Device driver and DMA controller synthesis from HW/SW communication protocol specifications. *Design Automation of Embedded Systems*, 6(2):177 – 207, April 2001.

[6] Ingo Sander, Axel Jantsch, and Zhonghai Lu. Development and application of design transformations in ForSyDe. *IEE Proceedings on Computers and Digital Technique*, 150(5):313–320, September 2003.

[7] Ingo Sander and Axel Jantsch. System modeling and transformational design refinement in ForSyDe. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 23(1):17–32, 1 2004.

[8] Axel Jantsch, Johnny Öberg, and Hannu Tenhunen. Special issue on networks on chip - guest editor's introduction. *Journal of Systems Architecture*, 50(2-3), February 2004.

[9] Dinesh Pamunuwa, Johnny Öberg, Li-Rong Zheng, Mikael Millberg, Axel Jantsch, and Hannu Tenhunen. A study on the implementation of 2-D mesh based networks on chip in the nanoregime. *Integration - The VLSI Journal*, 38(1):3–17, October 2004.

[10] Axel Jantsch and Ingo Sander. Models of computation and languages for embedded system design. *IEE Proceedings on Computers and Digital Tech-*

niques, 152(2):114–129, 3 2005. Special issue on Embedded Microelectronic Systems; Invited paper.

[11] Iyad Al Khatib, Davide Bertozzi, Francesco Poletti, Luca Benini, Axel Jantsch, Mohamed Bechara, Hasan Khalifeh, Mazen Hajjar, Rustam Nabiev, and Sven Jonsson. Hardware/software architecture for real-time ECG monitoring and analysis leveraging MPSoC technology. *Transactions on High-Performance Embedded Architectures and Compilers (HiPEAC)*, I(1):239–258, 2007. LNCS 4050.

[12] Deepak Mathaikutty, Hiren Patel, Sandeep Shukla, and Axel Jantsch. EWD: A metamodeling driven customizable multi-moc system modeling framework. *ACM Transactions on Design Automation of Embedded Systems*, 12(3), 8 2007.

[13] Zhonghai Lu and Axel Jantsch. Admitting and ejecting flits in wormhole-switched networks on chip. *IET Computers & Digital Techniques*, 5(1):546–556, September 2007.

[14] Deepak Mathaikutty, Hiren Patel, Sandeep Shukla, and Axel Jantsch. SML-Sys: A functional framework with multiple models of computation for modeling heterogeneous system. *Design Automation for Embedded Systems*, 12(1):1–30, 6 2008.

[15] Tarvo Raudvere, Ingo Sander, and Axel Jantsch. Application and verification of local non-semantic-preserving transformations in system design. *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, 27(6):1091–1103, 2008.

[16] Arseni Vitkovski, Axel Jantsch, Robert Lauter, Raimo Haukilahti, and Erland Nilsson. Low-pwer and error protection coding for network-on-chip traffic. *IET Computers and Digital Techniques*, 2(6):483–492, 2008.

[17] Ingo Sander and Axel Jantsch. Modelling adaptive systems in ForSyDe. *Electronic Notes in Theoretical Computer Science*, 200(2):39–54, February 2008.

[18] Iyad Al Khatib, Francesco Poletti, Davide Bertozzi, Luca Benini, Mohamed Bechara, Hasan Khalifeh, Axel Jantsch, and Rustam Nabiev. A multiprocessor system-on-chip for real-time biomedical monitoring and analysis: ECG prototype architectural design space exploration. *ACM Transactions on Design Automation of Embedded Systems*, 13(2), April 2008.

[19] Huimin She, Zhonghai Lu, Axel Jantsch, Li-Rong Zheng, and Dian Zhou. Analysis of traffic splitting mechanisms for 2D mesh sensor networks. *International Journal of Software Engineering and Its Applications (IJSEIA)*, 2(3), July 2008.

[20] Christoph Grimm, Axel Jantsch, Sandeep Shukla, and Eugenio Villar. C-based design of embedded systems - editorial. *EURASIP Journal on Embedded Systems*, July 2008.

[21] Zhonghai Lu and Axel Jantsch. TDM virtual-circuit configuration for network-on-chip. *IEEE Transactions on Very Large Scale Integration Systems*, 16(8), August 2008.

[22] Zhonghai Lu, Axel Jantsch, Erno Salminen, and Cristian Grecu. Network-on chip micro-benchmarks. *Embedded Systems Design*, September 2008.

[23] Tiberiu Seceleanu and Axel Jantsch. Modeling communication with synchronized environments. *Fundamenta Informaticae*, 86(3):343–369, October 2008.

[24] Abdul Naeem, Xiaowen Chen, Zhonghai Lu, and Axel Jantsch. Scalability of transaction counter based relaxed consistency models in NoC based multicore architectures. *ACM SIGARCH Computer Architecture News*, December 2009.

[25] Fahimeh Jafari, Zhonghai Lu, Axel Jantsch, and Mohammad Hossein Yaghmaee. Buffer optimization in network-on-chip through flow regulation. *IEEE Transactions on Computer Aided Design (TCAD)*, 29(12):1973–1986, December 2010.

[26] Xiaowen Chen, Zhonghai Lu, Axel Jantsch, Shuming Chen, and Hai Liu. Cooperative communication based barrier synchronization in on-chip mesh architectures. *IEICE Electronics Express*, 8(22):1856–1862, 2011.

[27] Iraklis Anagnostopoulos, Sotirios Xydis, Alexandros Bartzas, Zhonghai Lu, Dimitrios Soudris, and Axel Jantsch. Custom microcoded dynamic memory management for distributed on-chip memory organizations. *IEEE Embedded Systems Letters*, 2011.

[28] Ming Liu, Wolfgang Kuehn, Soeren Lange, Shua Yang, Johannes Roskoss, Zhonghai Lu, Axel Jantsch, Qiang Wang, Hao Xu, Dapeng Jin, and Zhenan Liu. A high-end reconfigurable computation platform for nuclear and particle physics experiments. *Computing in Science and Engineering*, 13(2):52–63, March-April 2011.

[29] Ming Liu, Zhonghai Lu, Wolfgang Kuehn, and Axel Jantsch. FPGA-based particle recognition in the HADES experiment. *Design and Test of Computers*, July-August 2011.

[30] Huimin She, Zhonghai Lu, Axel Jantsch, Dian Zhou, and Li-Rong Zheng. Performance analysis of flow based traffic splitting strategy on cluster-mesh sensor networks. *International Journal of Distributed Sensor Networks*, 2012.

[31] Abbas Eslami Kiasari, Axel Jantsch, and Zhonghai Lu. Mathematical formalisms for performance evaluation of networks-on-chip. *ACM Computing Surveys*, 2012. Accepted for Publication.

[32] Martin Radetzki, Chaochao Feng, Xueqian Zhao, and Axel Jantsch. Methods for fault tolerance in networks on chip. *Accepted for Pub-*

lication in ACM Computing Surveys, 2012. Availabfle for review at http://web.it.kth.se/~axel/papers/2013/FTNoC-Survey.pdf.

[33] Wenmin Hu, Hengzhu Liu, Zhonghai Lu, Axel Jantsch, and Guitao Fu. Self-selection pseudo-circuit: a clever crossbar pre-allocation. *IEICE Electronics Express*, 2012.

[34] Chaochao Feng, Zhonghai Lu, Axel Jantsch, Minxuan Zhang, and Xianju Yang. Support efficient and fault-tolerant multicast in bufferless network-on-chip. *IEICE Transactions on Information and Systems*, 2012.

[35] Jun Zhu, Ingo Sander, and Axel Jantsch. Performance analysis of reconfigurations in adaptive real-time streaming applications. *ACM Transactions in Embedded Computing Systems – Special issue on Embedded Systems for Real-time Multimedia*, 5 2012.

[36] Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen. Reducing virtual-to-physical address translation overhead in distributed shared memory based multi-core network-on-chips according to data property. *Computers and Electrical Engineering*, May 2012.

[37] Chaochao Feng, Zhonghai Lu, Axel Jantsch, and Minxuan Zhang. A 1-cycle 1.25GHz bufferless router for 3D network-on-chip. *IEICE Transactions on Information and Systems*, May 2012.

[38] Martin Radetzki and Axel Jantsch. Editorial introduction - special issue on languages, models and model based design for embedded systems. *Design Automation for Embedded Systems*, July 2012. Springer.

[39] Abbas Eslami Kiasari, Zhonghai Lu, and Axel Jantsch. An analytical latency model for networks-on-chip. *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, 21(1):113 –123, January 2013.

[40] Abdul Naeem, Axel Jantsch, and Zhonghai Lu. Scalability analysis of memory consistency models in NoC based distributed shared memory SoCs. *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, 32(5), May 2013.

Book Chapters

[1] Per Bjuréus and Axel Jantsch. Heterogenous system-level cosimulation with SDL and Matlab. In Jean Mermet, editor, *Electronic Chips & System Design Languages*, chapter 12, pages 145–157. Kluwer Academic Publisher, 2001.

[2] A. Jantsch, S. Kumar, I. Sander, B. Svantesson, J. Öberg, A. Hemani, Peeter Ellervee, and Mattias O'Nils. A comparison of six languages for system level description of telecom applications. In Jean Mermet, editor,

Electronic Chips & System Design Languages, chapter 15, pages 181–192. Kluwer Academic Publisher, 2001.

[3] Axel Jantsch and Hannu Tenhunen. Will networks on chip close the productivity gap? In Axel Jantsch and Hannu Tenhunen, editors, *Networks on Chip*, chapter 1, pages 3–18. Kluwer Academic Publishers, 2 2003.

[4] Martti Forsell, Juha-Pekka Soininen, Kari Tiensyriä, Axel Jantsch, Klaus Kronlöf, and Bojidar Hadjiski. Networks on chip: Approaches and challenges. In *Research and Development Activities in Telecommunication Systems*. VTT Electronics, 2004.

[5] Heiko Zimmer and Axel Jantsch. Error-tolerant interconnect schemes. In Jari Nurmi, Hannu Tenhunen, Jouni Isoaho, and Axel Jantsch, editors, *Interconnect-Centric Design for Advanced SoCs and NoCs*, chapter 6. Kluwer Academic Publisher, April 2004.

[6] Axel Jantsch. Models of embedded computation. In Richard Zurawski, editor, *Embedded Systems Handbook*. CRC Press, 2005. Invited contribution.

[7] Axel Jantsch and Ingo Sander. Models of computation in the design process. In Bashir M Al-Hashimi, editor, *SoC: Next Generation Electronics*. IEE, 2005. Invited contribution.

[8] Zhonghai Lu, Ingo Sander, and Axel Jantsch. Refining synchronous communication onto network-on-chip best-effort services. In Alain Vachoux, editor, *Advances in Design and Specification Languages for SoCs - Selected Contributions from FDL 2005*. Springer Verlag, 2006.

[9] Deepak Abraham Mathaikutty, Hiren Patel, Sandeep K. Shukla, and Axel Jantsch. UMoC++: A C++-based multi-MoC modeling environment. In Alain Vachoux, editor, *Advances in Design and Specification Languages for SoCs - Selected Contributions from FDL'05*, chapter 7. Springer Verlag, 2006.

[10] Axel Jantsch. Models of computation for distributed embedded systems. In Richard Zurawski, editor, *Networked Embedded Systems*. CRC Press/Taylor & Francis, 2009.

[11] Axel Jantsch and Zhonghai Lu. Resource allocation for quality of service in on-chip communication. In Fayez Gebali and Haytham Elmiligi, editors, *Networks on Chip: Theory and Practice*. Taylor & Francis Group LLC - CRC Press, 2009.

[12] Bernard Candaele, Sylvain Aguirre, Michel Sarlotte, Iraklis Anagnostopoulos, Sotirios Xydis, Alexandros Bartzas, Dimitris Bekiaris, Dimitrios Soudris, Zhonghai Lu, Xiaowen Chen, Jean-Michel Chabloz, Ahmed Hemani, Axel Jantsch, Geert Vanmeerbeeck, Jari Kreku, Kari Tiensyrja, Fragkiskos Ieromnimon, Dimitrios Kritharidis, Andreas Wiefrink, Bart Vanthournout, and Philippe Martin. The MOSART mapping optimiza-

tion for multi-core architectures. In *Designing Very Large Scale Integration Systems: Emerging Trends and Challenges*. Springer, 2011.

[13] Axel Jantsch, Xiaowen Chen, Abdul Naeem, Yuang Zhang, Sandro Penolazzi, and Zhonghai Lu. Memory architecture and management in an NoC platform. In Axel Jantsch and Dimitrios Soudris, editors, *Scalable Multi-core Architectures: Design Methodologies and Tools*. Springer, 2011.

[14] Axel Jantsch, Matthew Grange, and Dinesh Pamunuwa. The promises and limitations of 3-D integration. In Abbas Sheibanyrad, Frédéric Pétrot, and Axel Jantsch, editors, *3D Integartion for NoC-based SoC Architectures*, Integrated Circuits and Systems, chapter 2. Springer, 2011.

[15] Ming Liu, Zhonghai Lu, Wolfgang Kuehn, and Axel Jantsch. Adaptively reconfigurable controller for the flash memory. In *Book of Flash Memory*. InTech, 2011. ISBN: 978-953-307-272-2.

Conference Papers

[1] Axel Jantsch. A capability library for high level synthesis. In *Workshop on Control Dominated Synthesis*, 1992.

[2] Axel Jantsch. Hades: An environment for design space exploration. In *Proceedings of GME Fachtagung Mikroelektronik*, March 1993.

[3] Peeter Ellervee, Axel Jantsch, Johnny Öberg, Ahmed Hemani, and Hannu Tenhunen. Exploring asic design space at system level with a neural network estimator. In *7th Annual IEEE International ASIC Conference, ASIC'94*, 1994.

[4] Axel Jantsch, Peeter Ellervee, Johnny Öberg, and Ahmed Hemani. A case study on hardware/software partitioning. In *Proceedings of IEEE Workshop on FPGAs for Custom Computing Machines*, Napa, CA, April 1994.

[5] Axel Jantsch, Peeter Ellervee, Johnny Öberg, Ahmed Hemani, and Hannu Tenhunen. A software oriented approach to hardware/software codesign. In *Proceedings of the Poster Session of CC'94, International Conference on Compiler Construction*, Edinburgh, April 1994.

[6] Axel Jantsch, Peeter Ellervee, Johnny Öberg, Ahmed Hemani, and Hannu Tenhunen. Hardware-software partitioning and minimizing memory interface traffic. In *Proceedings of EURO-DAC '94*, Grenoble, France, September 1994.

[7] Axel Jantsch, Jouni Isoaho, and Johnny Öberg. Hardware-software codesign for multirate DSP system development. In *Poster session of Third International Workshop on Hardware-Software Codesign*, Grenoble, September 1994.

[8] Axel Jantsch and Jouni Isoaho. A versatile design validation environment by means of software execution, hardware simulation, and emulation. In *Proc. of the 36th SIMS Simulation Conference*, pages 322 – 325. Scandinavian Simulation Society, August 1994.

[9] Jouni Isoaho and Axel Jantsch. DSP development with full-speed prototyping based on HW-SW codesign techniques. In *Proc. of the Fourth International Workshop on Field programmable Logic and Applications, Prague, FPL'94*, September 1994.

[10] Peeter Ellervee, Johnny Öberg, Axel Jantsch, and Ahmed Hemani. Neural network based estimator to explore the design space at system level. In *Procceedings of the Biennial Baltic Electronic Conference, Tallin*, October 1994.

[11] J. Öberg, P. Ellervee, M. Mokhtari, and A. Jantsch. Design of a 1 gips peak performance processor using gaas technology. In *Proceedings of the IEEE NORCHIP Conference*, November 1994.

[12] J. Öberg, J. Isoaho, P. Ellervee, A. Jantsch, and A. Hemani. Babbage - a rule based tool for synthesis of hardware systems. In *Proceedings of the IEEE NORCHIP Conference*, November 1994.

[13] A. Hemani, B. Svantesson, P. Ellervee, A.Postula, J. Öberg, A.Jantsch, and H. Tenhunen. High-level synthesis of control and memory intensive communication systems. In *Proceedings of the 1995 ASIC Conference and Exhibit, Austin, Texas*, September 1995.

[14] Ahmed Hemani, Bengt Svantesson, Peeter Ellervee, Adam Postula, Axel Jantsch, and Hannu Tenhunen. Trade-offs in high-level synthesis of telecommunication circuits. In *Proceedings of SASIMI'95, Japan*, 1995.

[15] Johnny Öberg, Peeter Ellervee, Mehran Mokhtari, Axel Jantsch, and Ahmed Hemani. A 1 gips peak performance multi-threaded processor core using interleaved processing and a revolving register file targeted for gaas. In *5th Swedish Workshop on Computer System Architecture (DSA'95)*, 1995.

[16] T. Lazraq, B. Svantesson, A. Jantsch, and A. Hemani. Modelling of operation and maintance functions in the atm network. In *Proc. of the 9th European Simulation Multiconference*, June 1995.

[17] Mattias O'Nils, Axel Jantsch, Ahmed Hemani, and Hannu Tenhunen. Interactive hardware-software partitioning and memory allocation based on data transfer profiling. In *International Conference on Recent Advances in Mechatronics*, August 1995.

[18] Johnny Öberg, Jouni Isoaho, Peeter Ellervee, Axel Jantsch, and Ahmed Hemani. A rule-based approach for improving allocation of filter structures in hls. In *Proceedings of VLSI Design 96*, 1996.

[19] Kalle Tammemae, Mattias O'Nils, Axel Jantsch, and Ahmed Hemani. Hardware/software cosynthesis for reconfigurable systems. In *Proceedings of IEE Colloquium Hardware-Software Cosynthesis for Reconfigurable Systems*, February 1996.

[20] L. Hellberg, A. Hemani, J. Isoaho, A. Jantsch, M. Mokhtari, and H. Tenhunen. System oriented vlsi curriculum at kth. In *Proceedings of the International Conference on Microelectronic Systems Educations, MSE97*, 1997.

[21] L. Hellberg, A. Hemani, J. Isoaho, A. Jantsch, M. Mokhtari, and H. Tenhunen. Integration of physical and functional electronic system representations in electronic curriculum. In *Proceedings of the 15th NORCHIP Conference*, 1997.

[22] Axel Jantsch. Limitations of interactive design. In *Workshop on Electronic Design Processes*, 1997. http://www.cse.nd.edu/ cseda/edpw97/.

[23] Shashi Kumar, Axel Jantsch, Peeter Ellervee, Ahmed Hemani, and Anshul Kumar. Internal representation for specification and design of heterogenous systems. In *Third Workshop on Systems Design Languages, Italy*, July 1997.

[24] Axel Jantsch, Johann Notbauer, and Thomas Albrecht. Testcase development for large telecom systems. In *Proceedings of the International High-level Design Validation and test Workshop*, November 1997.

[25] Mattias O'Nils and Axel Jantsch. Communication in hardware/software embedded systems - a taxonomy and problem formulation. In *Proceedings of the 15th NORCHIP Conference*, November 1997.

[26] Peeter Ellervee, Shashi Kumar, Axel Jantsch, Bengt Svantesson, Thomas Meincke, and Ahmed Hemani. IRSYD: An internal representation for heterogeneous embedded systems. In *Proceedings of the 16th NORCHIP Conference*, 1998.

[27] Axel Jantsch, Johnny Öberg, and Ahmed Hemani. Is there a niche for a general protocol processor ? In *Proceeedings of 16th NORCHIP Conference*, 1998.

[28] A. Jantsch, S. Kumar, I. Sander, B. Svantesson, J. Öberg, and A. Hemani. Comparison of six languages for system level descriptions of telecom systems. In *Proceedings of the Forum on Design Languages*, volume 2, 1998.

[29] Mattias O'Nils, Johnny Öberg, and Axel Jantsch. Grammar based modelling and synthesis of device drivers and bus interfaces. In *Proceedings of the 24th Euromicro Conference, short contribution, Vasteras*, 1998.

[30] Johnny Oeberg, Axel Jantsch, and Ahmed Hemani. Validation of interface protocols using grammar-based models. In *Proceedings of the IEEE International High Level Design Validation and Test Workshop*, 1998.

[31] Johnny Öberg, Anshul Kumar, and Axel Jantsch. An object-oriented concept for intelligent library functions. In *Proceedings of the Eleventh International Conference on VLSI Design*, January 1998.

[32] Mattias O'Nils and Axel Jantsch. Multi-phase validation of hardware/software interfaces based on generated simulation models. In *Proceedings of the IEEE International High Level Design Validation and Test Workshop*, November 1998.

[33] Mattias O'Nils and Axel Jantsch. Refinement of HW/SW communication channels: Case study and comparison. In *Proceedings of the 16th NORCHIP Conference*, November 1998.

[34] Mattias O'Nils and Axel Jantsch. HW/SW interface validation in ip based system design. In *Proceedings of the International Workshop on IP Based Synthesis and System Design*, December 1998.

[35] Per Bjuréus and Axel Jantsch. Heterogenous system-level cosimulation with SDL and Matlab. In *Proceedings of the Forum on Design Languages (FDL)*, 1999.

[36] Wolfgang Horn, Bengt Svantesson, Shashi Kumar, Axel Jantsch, and Ahmed Hemani. Hardware synthesis of an atm multiplexer modelled in SDL: A case study. In *Proceedings of the IEEE Computer Society Annual Workshop on VLSI*, 1999.

[37] Axel Jantsch. Formal system specification models for verification and refinement. In *EDA-Traff'99*, 1999.

[38] Axel Jantsch. Integrated electronic systems program - a national research program. In *EDA-Traff'99*, 1999.

[39] Axel Jantsch, Shashi Kumar, and Ahmed Hemani. The Rugby model: A framework for the study of modelling, analysis, and synthesis concepts in electronic systems. In *Proceedings of Design Automation and Test in Europe (DATE)*, 1999.

[40] Thomas Meincke, Axel Jantsch, Peeter Ellervee, Ahmed Hemani, and Hannu Tenhunen. A generic scheme for communication representation and mapping. In *Proceedings of to IEEE Norchip Conference*, 1999.

[41] Mattias O'Nils and Axel Jantsch. Synthesis of DMA controllers from architecture independent descriptions of HW/SW communication protocols. In *Proceedings of the Twelfth International Conference on VLSI Design*, January 1999.

[42] Mattias O'Nils and Axel Jantsch. Operating system sensitive device driver synthesis from implementation independent protocol specification. In *Proceedings of Design Automation and Test in Europe*, 1999.

[43] Henrik Olson, Axel Jantsch, and Hannu Tenhunen. Floating- to fixed-point refinement in Matlab with an object-oriented library. In *Proceedings of the IEEE Norchip Conference*, 1999.

[44] Ingo Sander and Axel Jantsch. Formal design based on the synchronous approach, functional models and skeletons. In *Proceedings of the Twelfth International Conference on VLSI Design*, 1999.

[45] Ingo Sander and Axel Jantsch. System synthesis based on a formal computational model and skeletons. In *Proceedings of the IEEE Computer Society Annual Workshop on VLSI*, 1999.

[46] Ingo Sander and Axel Jantsch. System synthesis utilizing a layered functional model. In *Proceedings of the 7th International Workshop on Hardware/Software Codesign*, pages 136–141, May 1999.

[47] Per Bjuréus and Axel Jantsch. MASCOT: A specification and cosimulation method integrating data and control flow. In *Proceedings of the Design and Test Europe Conference (DATE)*, 2000.

[48] Axel Jantsch and Per Bjuréus. Composite signal flow: A computational model combining events, sampled streams, and vectors. In *Proceedings of the Design and Test Europe Conference (DATE)*, 2000.

[49] Axel Jantsch and Ingo Sander. On the roles of functions and objects in system specification. In *Proceedings of the International Workshop on Hardware/Software Codesign*, 2000.

[50] Yutai Ma, Axel Jantsch, and Hannu Tenhunen. A simple transition control for fsm programmable protocol processors. In *Proceedings of the 43rd Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2000.

[51] Patrick Schaumont, Mary Sheeran, Satnam Singh, and Axel Jantsch. Object oriented approach versus functional approach in system design. In *Proceedings of the Forum on Design Languages*, 2000.

[52] Johan Ditmar, Kjell Torkelsson, and Axel Jantsch. A dynamically reconfigurable fpga-based content addressable memory for internet protocol characterization. In Reiner W. Hartenstein and Herbert Grunbacher, editors, *Proceedings of the 10th International Conference on Field Programmable Logic and Applications*, volume 1896 of *Lecture Notes in Computer Science*, pages 19–28. Springer Verlag, August 2000.

[53] Wenbiao Wu, Ingo Sander, and Axel Jantsch. Transformational system design based on a formal computational model and skeletons. In *Proceedings of the Forum on Design Languages*, September 2000.

[54] Ahmed Hemani, Axel Jantsch, Shashi Kumar, Adam Postula, Johnny Öberg, Mikael Millberg, and Dan Lindqvist. Network on chip: An architecture for billion transistor era. In *Proceeding of the IEEE NorChip Conference*, November 2000.

[55] Yutai Ma, Axel Jantsch, and Hannu Tenhunen. A programmable protocol processor architecture for high speed internet protocol processing. In *Proceedings of the IEEE NORCHIP Conference*, November 2000.

[56] Yutai Ma, Axel Jantsch, and Hannu Tenhunen. A flexible register access control for programmable protocol processors. In *Proceedings of the 44th Midwest Symposium on Circuits and Systems (MWSCAS)*, August 2001.

[57] Axel Jantsch, Ingo Sander, and Wenbiao Wu. The usage of stochastic processes in embedded system specifications. In *Proceedings of the Ninth International Symposium on Hardware/Software Codesign*, April 2001.

[58] Axel Jantsch, Juha-Pekka Soininen, Martti Forsell, Li-Rong Zheng, Shashi Kumar, Mikael Millberg, and Johnny Öberg. Networks on chip. In *Workshop at the European Solid State Circuits Conference*, September 2001.

[59] Per Bjuréus and Axel Jantsch. Performance analysis with confidence intervals for embedded software processes. In *Proceedings of the International Symposium on System Synthesis (ISSS)*, October 2001.

[60] Abhijit K. Deb, Johnny Öberg, and Axel Jantsch. Control and communication performance analysis of embedded DSP systems in the MASIC methodology. In *Proceedings of the International Symposium on System Synthesis (ISSS)*, October 2001.

[61] Abhijit Kumar Deb, Johnny Oberg, and Axel Jantsch. Performance analsysi and architectural refinement of embedded DSP systems in the MASIC methodology. In *Proceedings of Swedish System-on-Chip Conference*, March 2002.

[62] Yutai Ma, Axel Jantsch, and Hannu Tenhunen. Load/store unit design of a programmable internet protocol processor. In *Proceedings of Swedish System-on-Chip Conference*, March 2002.

[63] Tarvo Raudvere, Ingo Sander, Ashish Kumar Singh, Dilian Gurov, and Axel Jantsch. The forsyde semantics. In *Proceedings of Swedish System-on-Chip Conference*, March 2002.

[64] Shashi Kumar, Axel Jantsch, Juha-Pekka Soininen, Martti Forsell, Mikael Millberg, Johnny Öberg, Kari Tiensyrjä, and Ahmed Hemani. A network on chip architecture and design methodology. In *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, April 2002.

[65] Per Bjureus, Mickael Millberg, and Axel Jantsch. FPGA resource and timing estimation from Matlab execution traces. In *Proceedings of the International Workshop on Hardware/Software Codesign*, May 2002.

[66] Tero Nurmi, Hannu Tenhunen, Li-Rong Zheng, Axel Jantsch, Jari Nurmi, and Jouni Isoaho. Physical performance modelling for platform-based SoC design. In *Proceedings of the 4th European Workshop on Microelectronics Education*, May 2002.

[67] Axel Jantsch. Network on chip. In *Proceedings of the Conference Radio vetenskap och Kommunication*, Stockholm, June 2002.

[68] Ingo Sander and Axel Jantsch. Transformation based communication and clock domain refinement for system design. In *Proceedings of Design Automation Conference*, June 2002.

[69] Yutai Ma, Axel Jantsch, and Hannu Tenhunen. Two special register addressing modes for internet protocol processing. In *Proc. of International Network Conference, Plymouth, United kingdom*, July 2002.

[70] Zhonghai Lu, Ingo Sander, and Axel Jantsch. A case study of hardware and software synthesis in ForSyDe. In *Proceedings of the 15th International Symposium on System Synthesis*, Kyoto, Japan, October 2002.

[71] Yi-Ran Sun, Shashi Kumar, and Axel Jantsch. Simulation and evaluation of a network on chip architecture using ns-2. In *Proceedings of the IEEE NorChip Conference*, November 2002.

[72] Juha-Pekka Soininen, Axel Jantsch, Martti Forsell, Antti Pelkonen, Jari Kreku, and Shashi Kumar. Extending platform-based design to network on chip systems. In *Proceedings of the International Conference on VLSI Design*, January 2003.

[73] Abhijit K. Deb, Johnny Öberg, and Axel Jantsch. Simulation and analysis of embedded DSP systems using MASIC methodology. In *Proceedings of the Design Automation and Test Europe (DATE)*, March 2003.

[74] Erland Nilsson, Mikael Millberg, Johnny Öberg, and Axel Jantsch. Load distribution with the proximity congestion awareness in a network on chip. In *Proceedings of the Design Automation and Test Europe (DATE)*, pages 1126–1127, March 2003.

[75] Ingo Sander, Axel Jantsch, and Zhonghai Lu. The development and application of formal design transformations in ForSyDe. In *Proceedings of the Design Automation and Test Europe (DATE)*, March 2003.

[76] Zhonghai Lu and Axel Jantsch. Refinement for communication-based design. In *Swedish System-on-Chip Conference (SSoCC'03)*, Eskilstuna, Sweden, April 2003.

[77] Abhijit K. Deb, Johnny Öberg, and Axel Jantsch. Simulation and analysis of embedded DSP systems using Petri nets. In *Proceedings of the 14th IEEE International Workshop on Rapid System Prototyping*, June 2003.

[78] Axel Jantsch. NoCs: A new contract between hardware and software. In *Proceedings of the Euromicro Symposium on Digital System Design*, September 2003. Invited keynote.

[79] Tarvo Raudvere, Ingo Sander, Ashish Kumar Singh, and Axel Jantsch. Verification of design decisions in forsyde. In *Proceedings of the CODES-ISSS Conference*, October 2003.

[80] Heiko Zimmer and Axel Jantsch. A fault model notation and error-control scheme for switch-to-switch buses in a network-on-chip. In *Proceedings of the CODES-ISSS Conference*, October 2003.

[81] Yutai Ma, Axel Jantsch, and Hannu Tenhunen. A group of subword instructions and design issues for network processing RISC cores. In *Proceedings of the IEEE NorChip Conference*, November 2003.

[82] Richard Thid, Mikael Millberg, and Axel Jantsch. Evaluating NoC communication backbones with simulation. In *Proceedings of the IEEE NorChip Conference*, November 2003.

[83] D. Pamunuwa, J. Öberg, L. R. Zheng, M. Millberg, A. Jantsch, and H. Tenhunen. Layout, performance and power trade-offs in mesh-based network-on-chip architectures. In *IFIP International Conference on Very Large Scale Integration (VLSI-SOC)*, Darmstadt, Germany, December 2003.

[84] Mikael Millberg, Erland Nilsson, Rikard Thid, Shashi Kumar, and Axel Jantsch. The Nostrum backbone - a communication protocol stack for networks on chip. In *Proceedings of the VLSI Design Conference*, Mumbai, India, January 2004.

[85] Abhijit K. Deb, Axel Jantsch, and Johnny Öberg. System design for dsp applications using the MASIC methodology. In *Proceedings of the Design Automation and Test Europe (DATE)*, February 2004.

[86] Mikael Millberg, Erland Nilsson, Rikard Thid, and Axel Jantsch. Guaranteed bandwidth using looped containers in temporally disjoint networks within the Nostrum network on chip. In *Proceedings of the Design Automation and Test Europe Conference (DATE)*, February 2004.

[87] Tarvo Raudvere, Ashish Kumar Singh, Ingo Sander, and Axel Jantsch. Polynomial abstraction for verification of sequentially implemented combinational circuits. In *Proceedings of the Design Automation and Test Europe Conference (DATE)*, February 2004. interactive presentation.

[88] Ingo Sander, Axel Jantsch, and Hannu Tenhunen. The platform as interface in a SoC design curriculum. In *Proceedings of te 5t European Worksop on Microelectronics Education*, April 2004.

[89] Abhijit K. Deb, Axel Jantsch, and Johnny Öberg. System design for dsp applications in transaction level modeling paradigm. In *Proc. Design Automation Conf. (DAC)*, pages 466–471, San Diego, California, June 2004.

[90] Zhonghai Lu and Axel Jantsch. Flit admission in on-chip wormhole-switched networks with virtual channels. In *Proceedings of the International Symposium on System-on-Chip 2003*, November 2004.

[91] Zhonghai Lu and Axel Jantsch. Flit ejection in on-chip wormhole-switched networks with virtual channels. In *Proceedings of the IEEE NorChip Conference*, November 2004.

[92] Arseni Vitkovski, Raimo Haukilahti, Axel Jantsch, and Erland Nilsson. Low-power and error coding for network-on-chip traffic. In *Proceedings of the IEEE NorChip Conference*, November 2004.

[93] Axel Jantsch, Robert Lauter, and Arseni Vitkowski. Power analysis of link level and end-to-end data protection on networks on chip. In *Proceedings of the IEEE International Symposium on Circuits and Systems*, 2005.

[94] Iyad Al Khatib, Axel Jantsch, and Mohammad Saleh. Simulation of real home healthcare sensor networks utilizing ieee 802.11g biomedical network-on-chip. In *Proceedings of REALWAN*, Stockholm, 2005.

[95] Zhonghai Lu, Axel Jantsch, and Ingo Sander. Feasibility analysis of messages for on-chip networks using wormhole routing. In *Proceedings of the Asian Pacific Design Automation Conference*, 2005.

[96] Deepak Abraham Mathaikutty, Hiren Patel, Sandeep K. Shukla, and Axel Jantsch. UMoC++: Modeling environment for heterogeneous systems based on generic MoCs. In *Proceedings of the Forum on Design Languages*, 9 2005.

[97] Iyad Al Khatib, Axel Jantsch, Bassam Kayal, Rustam Nabiev, and Sven Jonsson. Wireless network-on-chips as autonomous systems: A novel solution for biomedical healthcare and space exploration sensor-networks. In *Proceedings of the Infocom 2005 Conference - Student Workshop*, March 2005.

[98] Zhonghai Lu, Rikard Thid, Mikael Millberg, Erland Nilsson, and Axel Jantsch. NNSE: Nostrum network-on-chip simulation environment. In *Swedish System-on-Chip Conference (SSoCC'03)*, April 2005.

[99] Zhonghai Lu and Axel Jantsch. Traffic configuration for evaluating networks on chips. In *Proceedings of the 5th International Workshop on Systems on Chip (IWSOC)*, July 2005.

[100] Zhonghai Lu, Li Tong, Bei Yin, and Axel Jantsch. A power efficient flit-admission scheme for wormhole-switched networks on chip. In *Proceedings of the 9th World Multi-Conference on Systemics, Cybernetics and Informatics*, July 2005.

[101] Zhonghai Lu, Ingo Sander, and Axel Jantsch. Refinement of a perfectly synchronous communication model onto Nostrum NoC best-effort communication. In *Proceedings of the Forum on Design Languages*, September 2005.

[102] Tarvo Raudvere, Ashish K. Singh, Ingo Sander, and Axel Jantsch. System level verification of digital signal processing applications based on the polynomial abstraction technique. In *Proceedings of the Internatipnal Conference on Computer Aided Design (ICCAD)*, November 2005.

[103] Weixing Wang, Axel Jantsch, and Shuran Song. An algorithm of electing cluster head in beacon node distributions based on maximum residual energy. In *Proceedings of Annual Conference on Chinese Society of Agricultural Engineering*, volume 3:535-539, Guangzhou City, P. R. of China, December 2005.

[104] Iyad Al Khatib, Davide Bertozzi, Francesco Poletti, Luca Benini, Axel Jantsch, Mohamed Bechara, Hasan Khalifeh, Mazen Hajjar, Rustam Nabiev, and Sven Jonsson. MPSoC ECG biochip: A multiprocessor System-on-Chip for real-time human heart monitoring and analysis. In *Proceedings of the ACM Computing Frontiers*, 2006.

[105] Zhonghai Lu, Mingchen Zhong, and Axel Jantsch. Evaluation of onchip networks using deflection routing. In *Proceedings of GLSVLSI*, 2006.

[106] Jun Zhu, Axel Jantsch, and Ingo Sander. SDF to synchronous cross domain analysis in ForSyDe stream processing framework. In *2nd HiPEAC Industrial Workshop*, 10 2006.

[107] Zhonghai Lu, Bei Yin, and Axel Jantsch. Connection-oriented multicasting in wormhole-switched networks on chip. In *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, March 2006.

[108] Axel Jantsch. Models of computation for networks on chip. In *Proceedings of the Sixth International Conference on Application of Concurrency to System Design*, June 2006. invited paper.

[109] Tiberiu Seceleanu and Axel Jantsch. Communicating with synchronized environments. In *Proceedings of the Sixth International Conference on Application of Concurrency to System Design*, June 2006.

[110] Iyad Al-Khatib, Francesco Poletti, Davide Bertozzi, Luca Benini, Mohamed Bechara, Hasan Khalifeh, Axel Jantsch, and Rustam Nabiev. A multiprocessor system-on-chip for real-time biomedical monitoring and analysis: Architectural design space exploration. In *Proceedings of the Design Automation Conference*, July 2006.

[111] Weixing Wang and Axel Jantsch. A new protocol for electing cluster head based on maximum residual energy. In *Proceedings of the IEEE International Cross-Layer Designs and Protocols Symposium*, July 2006.

[112] Liang Guang and Axel Jantsch. Adaptive power management for the on-chip communication network. In *9th Euromicro Conference on Digital System Design (DSD 2006)*, August 2006.

[113] Zhonghai Lu, Ingo Sander, and Axel Jantsch. Towards performance-oriented pattern-based refinement of synchronous models onto NoC communication. In *9th Euromicro Conference on Digital System Design (DSD 2006)*, August 2006.

[114] Sandro Penolazzi and Axel Jantsch. A high level power model for the Nostrum NoC. In *9th Euromicro Conference on Digital System Design (DSD 2006)*, August 2006.

[115] Rikard Thid, Ingo Sander, and Axel Jantsch. Flexible bus and NoC performance analysis with configurable synthetic workloads. In *9th Euromicro Conference on Digital System Design (DSD 2006)*, August 2006.

[116] T. Seceleanu, A. Jantsch, and H. Tenhunen. On-chip distributed architectures. In *Proceedings of the IEEE International SOC Conference*, pages 329 – 330, September 2006.

[117] Ming Liu, Wolfgang Kuehn, Zhonghai Lu, Axel Jantsch, Shuo Yang, Tiago Perez, and Zhenan Liu. Hardware/software co-design of a general-purpose computation platform in particle physics. In *Proceedings of the ICFPT*, 2007.

[118] Tarvo Raudvere, Ingo Sander, and Axel Jantsch. A synchronization algorithm for local temporal refinements in perfectly synchronous models with nested feedback loops. In *Proceedings of the Great Lake Symposium on VLSI (GLSVLSI)*, 2007.

[119] Ingo Sander and Axel Jantsch. Modelling adaptive systems in ForSyDe. In *Proceedings of the First Workshop on Verification of Adaptive Systems (VerAS)*, pages 39–54, Kaiserslauten, 2007.

[120] Huimin She, Zhonghai Lu, Axel Jantsch, and Dian Zhou. A network-based system architecture for remote medical applications. In *Proceedings of the Asia-Pacific Advanced Network Meeting*, 2007.

[121] Andreas Herrholz, Frank Oppenheimer, Andreas Schallenberg, Wolfgang Nebel, Christoph Grimm, Markus Damm, Fernando Herrera, Eugenio Villar, Ingo Sander, Axel Jantsch, Anne-Marie Fouilliart, and Marcos Martinez. ANDRES - analysis and design of run-time reconfigurable, heterogeneous systems. In *Workshop on Reconfigurable Systems at DATE*, April 2007.

[122] Per Badlund and Axel Jantsch. An analytical approach for dimensioning mixed traffic networks. In *Proceedings of the 1st Symposium on Networks on Chip*, May 2007. poster.

[123] Andre Ivanov Cristian Grecu and, Partha Pande, Axel Jantsch, Erno Salminen, Umit Ogras, and Radu Marculescu. Towards open network-on-chip benchmarks. In *Proceedings of First International Symposium on Networks-on-Chip*, May 2007.

[124] Zhonghai Lu, Jonas Sicking, Ingo Sander, and Axel Jantsch. Using synchronizers for refining synchronous communication onto hardware/software architectures. In *Proceedings of the 18th IEEE/IFIP International Workshop on Rapid System Prototyping*, Porto Alegre, Brasil, May 2007.

[125] Mickael Millberg and Axel Jantsch. Improvements of performance and use of buffers in NoCs using dual packet exit. In *Proceedings of the 1st Symposium on Networks on Chip*, May 2007. poster.

[126] Zhonghai Lu, Ming Liu, and Axel Jantsch. Layered switching for networks on chip. In *Proceedings of the Design Automation Conference*, June 2007.

[127] Andreas Herrholz, Frank Oppenheimer, P. A. Hartmann, Andreas Schallenberg, Wolfgang Nebel, Christoph Grimm, Markus Damm, J. Haase, Fernando Herrera, Eugenio Villar, Ingo Sander, Axel Jantsch, Anne-Marie Fouilliart, and Marcos Martinez. The ANDRES project: Analysis and design of run-time reconfigurable, heterogeneous systems. In *Proceedings of the The International Conference on Field-Programmable Logic, Reconfigurable Computing, and Applications (FPL)*, August 2007.

[128] Mickael Millberg and Axel Jantsch. Increasing NoC performance and utilisation using a dualpacket exit strategy. In *10th Euromicro Conference on Digital System Design*, Lubeck, Germany, August 2007.

[129] Iyad Al-Khatib, Davide Bertozzi, Axel Jantsch, and Luca Benini. Performance analysis and design space exploration for high-end biomedical applications: Challenges and solutions. In *Proceedings of the International Conference on Hardware - Software Codesign and System Synthesis*, September 2007.

[130] Tarvo Raudvere, Ingo Sander, and Axel Jantsch. Synchronization after design refinements with sensitive delay elements. In *Proceedings of the International Conference on HW/SW Codesign and System Synthesis*, Salzburg, Austria, September 2007.

[131] Tomas Henriksson, Pieter van der Wolf, Axel Jantsch, and Alistair Bruce. Network calculus applied to verification of memory access performance in SoCs. In *Proceedings of the 5th IEEE Workshop on Embedded Systems for Real-Time Multimedia*, October 2007.

[132] Zhonghai Lu and Axel Jantsch. Slot allocation using logical networks for TDM virtual-circuit configuration for network-on-chip. In *International Conference on Computer Aided Design (ICCAD)*, November 2007.

[133] Huimin She, Zhonghai Lu, Axel Jantsch, Li-Rong Zheng, and Dian Zhou. Traffic splitting with network calculus for mesh sensor networks. In *Proceedings of the Future Generation Communication and Networking (FGCN)*, December 2007.

[134] Jun Zhu, Ingo Sander, and Axel Jantsch. Performance analysis of reconfiguration in adaptive real-time streaming applications. In *Proceedings of the 6th Workshop on Embedded Systems for Real-Time Multimedia (EstiMedia)*, Atlanta, USA, 10 2008.

[135] Jun Zhu, Ingo Sander, and Axel Jantsch. Energy efficient streaming applications with guaranteed throughput on MPSoCs. In *Proceedings of the International Conference on Embedded Software*, 10 2008.

[136] Zhonghai Lu, Lei Xia, and Axel Jantsch. Cluster-based simulated annealing for mapping cores onto 2d mesh networks on chip. In *Proceedings of the IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems*, April 2008.

[137] Huimin She, Zhonghai Lu, and Axel Jantsch. Deterministic worst-case performance analysis for wireless sensor networks. In *Proceedings of the International Wireless Communications and Mobile Computing Conference*, Crete, Greece, August 2008.

[138] Ming Liu, Wolfgang Kuehn, Zhonghai Lu, and Axel Jantsch. System-on-an-FPGA design for real-time particle track recognition and reconstruction in physics experiments. In *Proceedings of the Euromicro Diguital System Design Conference*, September 2008.

[139] Ming Liu, Tiago Perez, Johannes Lang, Shuo Yang, Wolfgang Kuehn, Hao Xu, Dapeng Jin, Qiang Wang, Lu Li, Zhen'An Liu, Zhonghai Lu, and Axel Jantsch. ATCA-based computation platform for data acquisition and triggering in particle physics experiments. In *Proceedings of the International Conference on Field Programmable Logic and Applications*, September 2008.

[140] Zhonghai Lu, Dimitris Brachos, and Axel Jantsch. A flow regulator for on-chip communication. In *Proceedings of the System on Chip Conference*, Belfast, Northern Ireland, 2009.

[141] Ingo Sander, Alfonso Acosta, and Axel Jantsch. Hardware design and synthesis in ForSyDe. In *Proceedings of Hardware Design and Functional Languages*, York, UK, 3 2009.

[142] Jun Zhu, Ingo Sander, and Axel Jantsch. Buffer minimization of real-time streaming applications scheduling on hybrid CPU/FPGA architectures. In *Proceedings of the Design and Test Europe Conference (DATE)*, 4 2009.

[143] Zhonghai Lu, Mikael Millberg, Axel Jantsch, Alistair Bruce, Pieter van der Wolf, and Tomas Henriksson. Flow regulation for on-chip communication. In *Proceedings of the Design Automation and Test Europe Conference (DATE)*, April 2009.

[144] Mikael Millberg and Axel Jantsch. Priority based forced requeue to reduce worst-case latency for bursty traffic. In *Proceedings of the Design Automation and Test Europe Conference (DATE)*, April 2009.

[145] Huimin She, Zhonghai Lu, Axel Jantsch, Dian Zhou, and Li-Rong Zheng. Analytical evaluation of retransmission schemes in wireless sensor networks. In *Proceedings of the IEEE 69th Vehicular Technology Conference: VTC2009-Spring*, April 2009.

[146] Yuang Zhang, Zhonghai Lu, Axel Jantsch, Li Li, and Minglun Gao. Towards hierarchical cluster based cache coherence for large-scale network-on-chip. In *Proceedings of the 4th IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era*, Cairo, Egypt, April 2009.

[147] Ming Liu, Axel Jantsch, Dapeng Jin, Andreas Kopp, Wolfgang Kuehn, Johannes Lang, Lu Li, Soeren Lange, Zhen'an Liu, Zhonghai Lu, David Muenchow, Vladimir Pechenov, Johannes Roskoss, Stephano Spataro, Qiang Wang, and Hao Xu. Trigger algorithm development on fpga-based compute nodes. In *16th IEEE NPSS Real Time Conference*, Beijing, May 2009.

[148] Ingo Sander, Jun Zhu, Axel Jantsch, Andreas Herrholzy, Philipp A. Hartmanny, and Wolfgang Nebel. High-level estimation and trade-off analysis for adaptive real-time systems. In *Proceedings of the 16th Reconfigurable Architectures Workshop*, Rome, May 2009.

[149] Qiang Wang, Axel Jantsch, Dapeng Jin, Andreas Kopp, Wolfgang Kuehn, Johannes Lang, Soeren Lange, Lu Li, Ming Liu, Zhen'an Liu, Zhonghai Lu, David Muenchow, Johannes Roskoss, and Hao Xu. Hardware/software co-design of an ATCA-based computation platform for data acquisition and triggering. In *16th IEEE NPSS Real Time Conference*, Beijing, May 2009.

[150] Awet Yemane Weldezion, Matt Grange, Dinesh Pamunuwa, Zhonghai Lu, Axel Jantsch, Roshan Weerasekera, and Hannu Tenhunen. Scalability of network-on-chip communication architecture for 3-d meshes. In *Proceedings of the International Symposium on Networks-on-Chip*, San Diego, CA, May 2009.

[151] Ming Liu, Wolfganga Kuehn, Zhonghai Lu, and Axel Jantsch. Run-time partial reconfiguration speed investigation and architectural design space exploration. In *Proceedings of the International Conference on Field Programmable Logic and Applications*, Prague, Chech Republic, September 2009.

[152] Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen. Speedup analysis of data-parallel applications on multi-core NoCs. In *Proceedings of the IEEE International Conference on ASIC (ASICON)*, Changsha, China, October 2009.

[153] Zhonghai Lu and Axel Jantsch. Trends of terascale computing chips in the next ten years. In *Proceedings of IEEE ASICON 2009*, ChangSha, China, October 2009.

[154] Ming Liu, Zhonghai Lu, Wolfgang Kuehn, Shuo Yang, and Axel Jantsch. A reconfigurable design framework for FPGA adaptive computing. In *Proceedings of the International Conference on ReConFigurable Computing and FPGAs*, Cancun, Mexico, December 2009.

[155] Jun Zhu, Ingo Sander, and Axel Jantsch. Pareto efficient design for reconfigurable streaming applications on CPU/FPGAs. In *Proceedings of Design Automation and Test in Europe (DATE '10)*, Dresden, Germany, 3 2010.

[156] Jun Zhu, Ingo Sander, and Axel Jantsch. Constrained global scheduling of streaming applications on MPSoCs. In *Proceedings of the conference on Asia South Pacific Design Automation (ASP-DAC '10)*, Taipei, Republic of China, 1 2010.

[157] Jun Zhu, Ingo Sander, and Axel Jantsch. HetMoC: Heterogeneous modeling in systemc. In *Proceedings of the Forum on Design Langauges (FDL)*, Southhampton, UK, 9 2010.

[158] Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen. Supporting distributed shared memory on multi-core network-on-chips using a dual microcoded controller. In *Proceedings of the confernece for Design Automation and Test in Europe*, Dresden, Germany, March 2010.

[159] Fahimeh Jafari, Zhonghai Lu, Axel Jantsch, and Mohammad H. Yaghmaee. Optimal regulation of traffic flows in networks-on-chip. In *Proceedings of the Design Automation and Test Europe Conference (DATE)*, Dresden, March 2010.

[160] Ming Liu, Zhonghai Lu, Wolfgang Kuehn, and Axel Jantsch. FPGA-based adaptive computing for correlated multi-stream processing. In *Proceedings of the Conference Design, Automation and Test Europe*, Dresden, Germany, March 2010.

[161] Amr Helmy, Laurence Pierre, and Axel Jantsch. Theorem proving techniques for formal verification of noc communications with non-minimal adaptive routing. In *Proceedings of the 13th IEEE International Symposium on Design & Diagnostics of Electronic Circuits & Systems*, Vienna, Austria, April 2010.

[162] Ming Liu, Zhonghai Lu, Wolfgang Kuehn, and Axel Jantsch. Reducing FPGA reconfiguration time overhead using virtual configurations. In *Proceedings of the 5th International Workshop on Reconfigurable Communication Centric Systems-on-Chip*, Karlsruhe, Germany, May 2010.

[163] Abdul Naeem, Xiaowen Chen, Zhonghai Lu, and Axel Jantsch. Scalability of weak consistency in NoC based multicore architectures. In *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Paris, France, June 2010.

[164] Bernard Candaele, Sylvain Aguirre, Michel Sarlotte, Iraklis Anagnostopoulos, Sotirios Xydis, Alexandros Bartzas, Dimitris Bekiaris, Dimitrios Soudris, Zhonghai Lu, Xiaowen Chen, Jean-Michel Chabloz, Ahmed Hemani, Axel Jantsch, Geert Vanmeerbeeck, Jari Kreku, Kari Tiensyrja, Fragkiskos Ieromnimon, Dimitrios Kritharidis, Andreas Wiefrink, Bart Vanthournout, and Philippe Martin. Mapping optimisation for scalable

multi-core architecture: The MOSART approach. In *Proceedings of the IEEE Annual Symposium on VLSI*, Kefalonia, Greece, July 2010.

[165] Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen. Supporting efficient synchronization in multi-core NoCs using dynamic buffer allocation technique. In *Proceedings of the IEEE Annual Symposium on VLSI*, Kefalonia, Greece, July 2010.

[166] Ming Liu, Zhonghai Lu, Wolfgang Kuehn, and Axel Jantsch. Inter-process communication using pipes in FPGA-based adaptive computing. In *Proceedings of the IEEE Annual Symposium on VLSI*, Kefalonia, Greece, July 2010.

[167] Xiaowen Chen, Zhonghai Lu, Axel Jantsch, and Shuming Chen. Handling shared variable synchronization in multi-core network-on-chip with distributed memory. In *International SOC Conference*, Las Vegas, Nevada, September 2010.

[168] Zhipeng Chen and Axel Jantsch. A worst case performance model for TDM virtual circuit in nocs. In *Proceedings of the International Workshop on Network on Chip*, Zheng Zhou, China, September 2010.

[169] Chaochao Feng, Zhonghai Lu, Axel Jantsch, Jinwen Li, and Minxuan Zhang. FoN: Fault-on-neighbor aware routing algorithm for networks-on-chip. In *International SOC Conference*, Las Vegas, Nevada, September 2010.

[170] Xiaowen Chen, Shuming Chen, Zhonghai Lu, and Axel Jantsch. Area and performance optimization of barrier synchronization on multi-core network-on-chips. In *3rd IEEE International Conference on Computer and Electrical Engineering (ICCEE)*, Chengdu, China, November 2010.

[171] Xiaowen Chen, Shuming Chen, Zhonghai Lu, and Axel Jantsch. Multi-FPGA implementation of a network-on-chip based many-core architecture with fast barrier synchronization mechanism. In *Proceedings of the IEEE Norchip Conference*, Tampere, Finland, November 2010.

[172] Chaochao Feng, Zhonghai Lu, Axel Jantsch, Jinwen Li, and Minxuan Zhang. A reconfigurable fault-tolerant deflection routing algorithm based on reinforcement learning for networks-on-chip. In *Proceedings of the International Workshop on Network on Chip Architectures (NoCArc)*, Atlanta, Gorgia, November 2010.

[173] Abbas Eslami Kiasari, Axel Jantsch, and Zhonghai Lu. A framework for designing congestion-aware deterministic routing. In *Proceedings of the International Workshop on Network on Chip Architectures (NoCArc)*, Atlanta, Gorgia, November 2010.

[174] Xiaowen Chen, Zhonghai Lu, Shuming Chen, and Axel Jantsch. Run-time partitioning of hybrid distributed shared memory on multi-core network-on-chips. In *The 3rd IEEE International Symposium on Parallel Architec-*

tures, Algorithms and Programming (PAAP 2010), Dalian, China, December 2010.

[175] Wenmin Hu, Zhonghai Lu, Axel Jantsch, and Hengzhu Liu. Power-efficient tree-based multicast support for networks-on-chip. In *Proceedings of the Asian Pacific Design Automation Conference (ASPDAC)*, Tokyo, Japan, January 2011.

[176] Abdul Naeem, Xiaowen Chen, Zhonghai Lu, and Axel Jantsch. Realization and performance comparison of sequential and weak memory consistency models in network-on-chip based multi-core systems. In *Proceedings of the 16th Asian Pacific Design Automation Conference (ASP-DAC)*, Tokyo, Japan, January 2011.

[177] Ming Liu, Zhonghai Lu, Wolfgang Kuehn, and Axel Jantsch. FPGA-based cherenkov ring recognition in nuclear and particle physics experiments. In *Proceedings of the 7th International Symposium on Applied Reconfigurable Computing*, belfast, UK, March 2011.

[178] Huimin She, Zhonghai Lu, Axel Jantsch, Dian Zhou, and Li-Rong Zheng. Modeling and analysis of rayleigh fading channels using stochastic network calculus. In *Proceedings of IEEE Wireless Communication and Networking Conference (WCNC2011*, Mexico, April 2011.

[179] Matt Grange, Roshan Weerasekera, Dinesh Pamunuwa, Axel Jantsch, and Awet Yemane Waldezione. Optimal network architectures for minimizing average distance in k-ary n-dimensional mesh networks. In *Proceedings of the Networks on Chip Symposium (NoCS)*, Pittsburgh, Pennsylvania, USA, May 2011.

[180] Chaochao Feng, Zhonghai Lu, Axel Jantsch, Minxuan Zhang, Jinwen Li, and Jiang Jiang. A low-overhead fault-aware deflection routing algorithm for 3D network-on-chip. In *Proceedings of the IEEE Annual Symposium on VLSI (ISVLSI)*, Chennai, India, July 2011.

[181] Meganathan Deivasigamani, Shaghayeghsadat Tabatabaei, Naveed Mustafa, Hamza Ijaz, Haris Bin Aslam, Shaoteng Liu, and Axel Jantsch. Concept and design of exhaustive-parallel search algorithm for Network-on-Chip. In *Proceedings of the International SoC Conference*, pages 150–155, September 2011.

[182] Abdul Naeem, Axel Jantsch, Xiaowen Chen, and Zhonghai Lu. Realization and scalability of release and protected release considtency models in noc based systems. In *Proceedings of the Euromicro Conference on Digital Systems Design (DSD)*, Oulu, Finland, September 2011.

[183] Huimin She, Zhonghai Lu, Axel Jantsch, Dian Zhou, and Li-Rong Zheng. Stochastic coverage in event-driven sensor networks. In *Proceedings of the IEEE Symposium on Personal, Indoor, Mobile and Radio Communications (PIMRC)*, Toronto, Canada, September 2011.

[184] Chaochao Feng, Jinwen Li, Zhonghai Lu, Axel Jantsch, and Minxuan Zhang. Evaluation of deflection routing on various NoC topologies. In *Proceedings of the IEEE International Conference on ASIC (ASICON)*, Xiamen, China, October 2011.

[185] Dinesh Pamunuwa, Matthew Grange, Roshan Weerasekera, and Axel Jantsch. 3-D integration and the limits of silicon computation. In *Proceedings of the International Conference on Very Large Scale Integration (VLSI-SoC)*, Hong Kong, October 2011. Invited Talk.

[186] Wenmin Hu, Zhonghai Lu, Axel Jantsch, Hengzhu Liu, Botao Zhang, and Dongpei Liu. Network-on-chip multicasting with low latency path setup. In *Proceedings of the VLSI-SoC Conference*, October 2011.

[187] Fahimeh Jafari, Axel Jantsch, and Zhonghai Lu. Output process of variable bit-rate flows in on-chip networks based on aggregate scheduling. In *Proceedings of the International Conference on Computer Design*, Amherst, Massachusetts, USA, October 2011.

[188] Matt Grange, Axel Jantsch, Roshan Weerasekera, and Dinesh Pamunuwa. Modeling the computational efficiency of 2-D and 3-D silicon processors for early-chip planning. In *Proceedings of the International Conference on CAD (ICCAD)*, San Jose, CA, USA, November 2011.

[189] Huimin She, Zhonghai Lu, and Axel Jantsch. System-level evaluation of sensor networks deployment strategies: Coverage lifetime and cost. In *Proceedings of the 8th International Wireless Communications and Mobile Computing Conference*, 2012.

[190] Syed M. A. H. Jafri, Liang Guang, Axel Jantsch, Kolin Paul, Ahmed Hemani, and Hannu Tenhunen. Self-adaptive NoC power management with dual-level agents: Architecture and implementation. In *Proceedings of the Conference on Self-adaptive Netwotrked Embedded Systems*, Rome, Italy, February 2012.

[191] Huimin She, Zhonghai Lu, Axel Jantsch, and Li-Rong Zheng. Estimation of statistical bandwidth through backlog measurement. In *Workshop on Network Calculus (WoNeCa2012)*, March 2012.

[192] Shaoteng Liu, Axel Jantsch, and Zhonghai Lu. Parallel probing: Dynamic and constant time setup procedure in circuit switching NoCs. In *Proceedings of the Design and Test in Europe Conference (DATE)*, Dresden, Germany, March 2012.

[193] Fahimeh Jafari, Axel Jantsch, and Zhonghai Lu. Worst-case delay analysis of variable bit-rate flows in network-on-chip with aggregate scheduling. In *Proceedings of the Design and Test in Europe Conference (DATE)*, Dresden, Germany, March 2012.

[194] Abdul Naeem, Axel Jantsch, and Zhonghai Lu. Architecture support and comparison of three memory consistency models in noc based systems. In

Proceedings of the Euromicro Conference on Digital Systems Design (DSD), Izmir, Turkey, September 2012.

[195] Abdul Naeem, Axel Jantsch, and Zhonghai Lu. Scalability analysis of release and sequential consistency models in noc based multicore systems. In *Proceedings of the International Symposium on Systems on Chip*, Tampere, Finland, October 2012.

[196] Shaoteng Liu, Axel Jantsch, and Zhonghai Lu. Comparison of circuit switched NoC with packet switched NoC. In *Fifth Swedish Workshop on Multicore Computing*, Stockholm, Sweden, November 2012.

[197] Rajeev Kumar Kanth, Pasi Liljeberg, Hannu Tenhuen, Qiang Chen, Axel Jantsch, Lirong Zheng, Harish Kumar, Leena Varshney, and Vibha Rani. Design of sierpinski grid patch antenna for multiband application and sustainability analysis in its manufacturing process. In *Proceedings of the International Conference on Industrialk Technology*, Cape Town, South Africa, February 2013.