Axel Jantsch - Short CV

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1 Personal facts

Full name: Axel Arthur Jantsch
Born in Klagenfurt, Austria, on December 20, 1962.
Married since April 1988; 2 children.
Current position: Professor in Electronic Systems Design and Head of the Department of Electronic Systems, Royal Institute of Technology, Stockholm, Sweden.
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2 Research interests

Embedded systems and dependable systems
Modeling concepts and languages
Systems on Chip architecture and design
Design methodology and tools

3 Education

January 1988:	Dipl.Ing. in Informatik (Master), Vienna University of Technology.
December 1992:	Dr. Tech. in Computer Science (PhD), Vienna University of Technology.
June 2000:	Docent of the Royal Institute of Technology.
December 2010:	Docent at the University of Turku, Finland.

4 Positions and employments

4.1 Employments

March 1988 - February 1993:	Research and teaching assistant at TU Vienna.
April 1993 - March 1995:	Postdoc at KTH Royal Institute of Technology, Stockholm, Sweden.
June 1995 - December 1996:	Siemens Austria AG in Vienna.
Since 1996:	Royal Institute of Technology (KTH), Stockholm, Sweden; (Associate professor since 1997, full professor since 2002, head of department since 2009).

4.2 Academic positions

April 1993 - March 1995:	Postdoc at KTH Royal Institute of Technology, Stockholm, Sweden.
January 1997:	Univ lektor (Associate Professor) at KTH.
June 2000:	Docent of the Royal Institute of Technology.
December 2002:	Full professor in Electronic System Design at KTH.
March 2007-June 2007:	Guest Professor at TU Vienna.
December 2007:	Guest Professor at Fudan University, Shanghai, China.
June 2009:	Guest Professor at Fudan University, Shanghai, China.
December 2010:	Docent at the University of Turku, Finland.
2011-2012:	Guest professor at the Chinese Academy of Science in Shenzhen, China.

4.3 Leadership in research and education programs

January 1999 - December 2002:	Program director of the Foundation for Strategic Research (SSF) funded national research program Integrated Electronic Systems (INTELECT), with a duration of four years and a budget of 110 M SEK ($\tilde{1}$2 M Euro).
October 2006-June 2009:	Responsible director for the international Master Program System on Chip Design".
April 2011 - September 2012:	Coordinator of the EIT ICTLabs (www.eitictlabs.eu) Master program in Embedded Systems with participating schools: KTH, TU Eindhoven, TU Berlin, U of Trento, U of Turku, Aalto University.
Since June 2012:	Director of iPack Excellence Center, funded by Vinnova with a 3 years budget of 66 Mkr (ca. 8 M Euro) and 13 partner companies.

4.4 Industrial positions

1983 - 1988:	Development of financial software and accounting systems as part time employment at Schellenberger GmbH, Vienna.
June 1995 - December 1996:	Siemens Austria AG in Vienna.
Since September 2005:	Member of the Steering Board at FrameAccess AB.
Since September 1010:	Co-founder and Member of the Steering Board of ELSIP AB.
Since January 1012:	founder and Member of the Steering Board of Memcom.Soc Ltd.

5 Other Professional Activities

I have served as TPC member, steering group member, and TPC chair, general chair and in various others operational roles for conferences like DATE, CODES-ISSS, NoCS, FDL, DCC, SoC Symposium, and others, since 1998.
I have been subject area editor for Journal of Systems Architecture from 2002-2008, and have served as reviewer and guest editor for many journals, e.g. IEEE TVLSI, IEEE TCAD, IEEE T Circuits and Systems, DAES, Desgign & Test, IEEE Computer, ACM TECS, IEEE TPDS, IEEE Transactions on Computers, etc.
I have served as reviewer of projects for the Dutch Technology Foundation, the Academy of Finland, the Engineering and Physical Science Research Council in UK, Sweden's VR, EU FP7, Artemis, ERC, and others.

6 Awards

Best paper nomination at the Forum on Design Languages, 1999.
Best paper award at the 10th International Conference on Field Programmable Logic and Applications, August 2000.
Best paper nomination at the Design Automation and Test in Europe Conference 2003.
Best paper nomination at the Design Automation and Test in Europe Conference 2004.
Best paper nomination at the Design Automation Conference (DAC) 2006.

7 Invited Talks and Seminars

I have given over 100 invited talks, seminars, key-notes, and tutorials at international conferences, summer schools, at universities and in industry.

8 Main Research Contributions

Development of a HW/SW codesign system, named Akka, as a post doctoral scholar at KTH, 1993-1995. The main contributions were a partitioning algorithm based on dynamic programming, a cosimulation environment, a coemulation environment, a profiling method for performance estimation, and a graphical front-end to visualize design properties. This activity eventually led to 1 Licentiate thesis, 1 PhD thesis, a few Master theses, and initiated the HW/SW codesign activity at the Royal Institute of Technology.

Development of a **formal framework for models of computation** that is based on deterministic process networks. Based on the concepts described in *Modeling Embedded Systems and SoCs - Concurrency and Time in Models of Computation*, Morgan Kaufmann Publishers, June 2003, the ForSyDe modelling and design methodology has been developed together with Ph.D. students Ingo Sander, Wenbiao Wu, Tarvo Raudvere, Ashish Singh, Zhonghai Lu, Jun Zhu at the Royal Institute of Technology. Since then Ingo Sander has become Associate Professor and is now leadiong this research activity.
Development of **Nostrum**, the KTH Network on Chip together with Ahmed Hemani, Shashi Kumar, Zhonghai Lu, Mikael Millberg, Erland Nilsson, Richard Thid, Johnny Öberg and others. Nostrum is based on a buffer-less, loss-less minimal switch architecture that offers both best effort and guaranteed bandwidth services. Starting in the year 2000 this activity was among the first and pioneering research in the NoC field.
Development of **McNoC**, an on-chip distributed shared memory architecture based on our Nostrum NoC. Based on the observation that the memory access bottleneck is becoming more and more severe, and on the prospect that 3D integration will allow the integration of massive amounts of DRAM into a stacked system with very high memory bandwidth for each individual core, we started to develop a DSM (Distributed Shared Memory) architecture. At the centre of this architecture is a programmable controller, called the DME (Data Management Engine), that can realize virtual-to-physical address translation, cache coherence protocols, memory consistency models and dynamic memory allocation algorithms in microcode. So far this work has resulted in a number of publications, a patent submission and industrial collaboration with ST Microelectronics in Grenoble and Huawei in Sweden and Shanghai, and in 2 spin-off companies (ELSIP in 2010, Memcom in 2012).
Development of a **compositional performance analysis method** for SoCs and embedded systems. This method is based on Network Calculus and allows for worst case timing analysis, dimensioning of platform resources and for traffic shaping. This method is also applied in wireless sensor networks. In 2011 this activity has resulted in a cooperation project with Intel. My former Ph.D. student has become Associate Professor and is now leading this effort.

9 Experience in Management

January 1999-December 2002 I was general manager of SSF's (Stiftelsen för strategisk forskning) program *Integrated Electronic System*s, which involves groups from four Universities (KTH, LiTH, LTH, CTH) and has a four year budget of 110 MSEK (€13 M).
January 2004-September 2005 I was head the Laboratory for Electronics and Computer Systems (LECS), which hosted 8 professors and in total 65 persons. As head I had financial and personell responsibility.
Since July 2009 I am head of the Electronic Systems Department with 60 persons and a yearly budget of 40 MSEK (€4.7 M).
Since June 2012 I am director of the iPack excellence center, which is ten years research program funded by Vinnova with a yearly budget of 22 MSEK (€2.6 M).

10 Teaching Experience

I have contributed or coordinated the development of the SoC Master program at KTH, a joint KTH-Fudan SoC master program, the Embedded Systems Master program at KTH, the Embedded Systems master program at Jönköping University, the EIT Master program on Innovation with specialization in Embedded Systems.
I have taught 8 difference courses on SoC architecture, embedded systems, system modeling, concurrent engineering, embedded systems design, in total 36 times. Most of these courses I have defined and developed myslef entirely or to a large extent.
I have supervised or examined 110 master theses.
I have co-authored 4 publications on education and given 5 invited seminars and talks on educational topics.
I have supervised and graduated 12 Ph.D. students.
I have served as expert or in the grading committee for 36 Ph.D. students.

11 Grants and research contracts

Project name	Period	Funding Agency	Amount	Note
Schrödinger Scholarship	1993-1995	Austrian Science Foundation	ÖS 600 k	
AASIC Consortium	1997-1999	SSF (Strategic Research Foundation)	SEK 2.5 M	Industrial participation
SAVE	1998-2000	NUTEK	SEK 1.3 M	50% industrial cofunding
MASCOT	1998-2002	SaabTech	SEK 600 k	+ fulltime Ph.D. student
ArchDes	1999-2000	Jönköping School of Engineering	SEK 400 k	+ fulltime Ph.D. student
Protocol Processor	1999-2002	SSF/Intelect	SEK 2.4 M	Industrial participation
MASIC	1999-2002	SSF/Intelect	SEK 1.8 M	Industrial participation
Low Power Operating Systems	2000-2003	SSF/Intelect	SEK 1.8 M	Industrial participation
System Specification and Verification	2001-2003	SSF/Intelect	SEK 1.2 M	Industrial participation
Formal System Design	1999-2003	SSF/Intelect	SEK 1.6 M	Industrial participation
NOCARC	2001-2003	Vinnova	SEK 3 M	50% industrial cofunding
NOC Design Methodology	2001-2004	SOCWare	SEK 2.25 M	Industrial participation
NOC Evaluation	2002-2005	SOCWare	SEK 1.5 M	Industrial participation
SOC-SME	2002-2004	Nordisk Industri Fond	NOK 900 k	50% cofunding
SOC-Mobinet	2002-2004	EU	€870 k	50% industrial cofunding;Main applicant: H. Tenhunen
SaverNOC	2005-2007	SaabTech	SEK 360 k	+ fulltime Ph.D. student
SPRINT	2006-2008	EU	€304 k	IP project, Philips Semiconductor is coordinator
ANDRES	2006-2008	EU	€223 k	STREP project, OFFIS is coordinator
HET-MoC	2006-2008	Swedish Research Council	SEK 2.2 M	
MOSART	2008-2011	EU	€247 k	STREP project, Thales is coordinator
SYSMODEL	2009-2011	EU Artemis	€360 k	
NoC ADM	2009-2011	Swedish Resarch Council	SEK 2.4 M	
NoC Evaluation	2010-2011	Huawei Sweden AB	SEK 1.5 M	
iFEST	2010-2013	EU Artemis	€300 k	ABB is coordinator
DME Verification	2010-2013	Vinnova	SEK 2 M	Research commercialization project
NoC Performance Analysis	2011-2013	Intel Inc in USA	US$ 300 k	
iPack Excellence Center	2013-2016	Vinnova	SEK 66 M	10 year center; decision taken for 3 years; 13 companies with cofunding;

12 Peer reviewed publications

Between 1992 and 2013 I have published over 250 peer reviewed contributions:
197 papers in international conferences
40 journal articles
15 book chapters
5 books as editor
1 book as author
Citations on Google Scholar: Total: 5688, h-index: 27, i10-index: 91, highest cited paper: 1014.